

Gallium Nitride E-Mode HEMT

GS700EWF250G1: 250mΩ, 700V



Description

This is a 700V GaN-on-Si enhancement-mode power transistor. The properties of GaN allow for high current, high breakdown voltage and high switching frequency.

Features

- Ultra-low FOM
- Ultra-high switching frequency
- Reverse current capability
- Zero reverse recovery loss
- Monolithic integrated ESD protection
- RoHS, Pb-free, REACH-compliant

Applications

- AC/DC converters
- DC/DC converters
- Bridgeless totem pole PFC
- Fast chargers
- Power adapters
- LED lighting drivers
- Wireless power transfer
- Laser drivers
- TV display

Table 1 Key Performance Parameters at T_j = 25 °C

Parameters	Values	Units
V _{DS, max}	700	V
R _{DS(on), Typ}	250	mΩ
Q _G	1.5	nC
I _{D, Pulse}	10	A
Q _{OSS @ 400 V}	13	nC
Q _{rr}	0	nC

Table2 Ordering Information

Ordering Code	Package	Product code
GS700EWF250G1	Wafer	GS700EWF250G1

Table of contents

Features.....	1
Applications.....	1
Table of contents.....	2
1 Maximum ratings.....	3
2 Electrical characteristics.....	4
3 Electrical characteristics diagrams.....	6
4 Chip Information.....	12
5 Wafer Information.....	13
6 Bonding Information.....	14
7 Revision history.....	15

1 Maximum ratings

at $T_j = 25\text{ °C}$ unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime.

Table 3 Maximum rating

Parameters	Symbols	Values	Units	Notes/Test Conditions
Drain-source voltage	$V_{DS, max}$	700	V	$V_{GS} = 0\text{ V}$ $T_j = -55\text{ °C to }150\text{ °C}$
Drain-source voltage transient ¹	$V_{DS, transient}$	800	V	$V_{GS} = 0\text{ V}$
Continuous current, drain-source	I_D	6	A	$T_c = 25\text{ °C}$
Pulsed current, drain-source ²	$I_{D, pulse}$	10	A	$T_c = 25\text{ °C}; V_G = 6\text{ V}$
Pulsed current, drain-source ²	$I_{D, pulse}$	6	A	$T_c = 125\text{ °C}; V_G = 6\text{ V}$
Gate-source voltage, continuous	V_{GS}	-1 to +6	V	$T_j = -55\text{ °C to }150\text{ °C}$
Gate-source voltage, pulsed	$V_{GS, pulse}$	-20 to +10	V	$T_j = -55\text{ °C to }150\text{ °C};$ $t_{Pulse} = 50\text{ ns}, f = 100\text{ kHz};$ open drain
Power dissipation	P_{tot}	50	W	$T_c = 25\text{ °C}$
Operating temperature	T_j	-55 to +150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, $t_{Pulse} < 1\text{ }\mu\text{s}$.

2. Pulse width = 10 μs .

2 Electrical characteristics

at $T_j = 25\text{ }^{\circ}\text{C}$, unless specified otherwise.

Table 4 Static characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.0	1.6	2.5	V	$I_D = 6\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	2	-		$I_D = 6\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 150\text{ }^{\circ}\text{C}$
Drain-source leakage current	I_{DSS}	-	0.01	0.6	μA	$V_{DS} = 700\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	0.6	-		$V_{DS} = 700\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	2	-	μA	$V_{GS} = 6\text{ V}$; $V_{DS} = 0\text{ V}$
Drain-source on-state Resistance ¹	$R_{DS(on)}$	-	250	310	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 2.2\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	590	-	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 2.2\text{ A}$; $T_j = 150\text{ }^{\circ}\text{C}$
Gate resistance	R_G	-	11	-	Ω	$f = 5\text{ MHz}$; open drain

1. $R_{DS(on)}$ is the test of fresh devices

Table 5 Dynamic characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	50	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ KHz}$
Output capacitance	C_{oss}	-	15	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ KHz}$
Reverse transfer capacitance	C_{rss}	-	0.2	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ KHz}$
Effective output capacitance, energy related ¹	$C_{o(er)}$	-	17	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related ²	$C_{o(tr)}$	-	24	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Output charge	Q_{oss}	-	11	-	nC	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	0.9	-	ns	$V_{DS} = 400\text{ V}$; $I_D = 4.4\text{ A}$; $L = 318\text{ }\mu\text{H}$; $V_{GS} = 6\text{ V}$; $R_{on} = 10\text{ }\Omega$; $R_{off} = 2\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	1.2	-	ns	
Rise time	t_r	-	3.5	-	ns	
Fall time	t_f	-	6.1	-	ns	

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.

2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V.

Table 6 Gate charge characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	Q_G	-	1.5	-	nC	$V_{GS} = 0 \text{ to } 6 \text{ V}; V_{DS} = 400 \text{ V};$ $I_D = 2.2 \text{ A}$
Gate-source charge	Q_{GS}	-	0.15	-	nC	
Gate-drain charge	Q_{GD}	-	0.5	-	nC	
Gate plateau voltage	V_{plat}	-	2.5	-	V	$V_{DS} = 400 \text{ V}; I_D = 2.2 \text{ A}$

Table 7 Reverse conduction characteristics

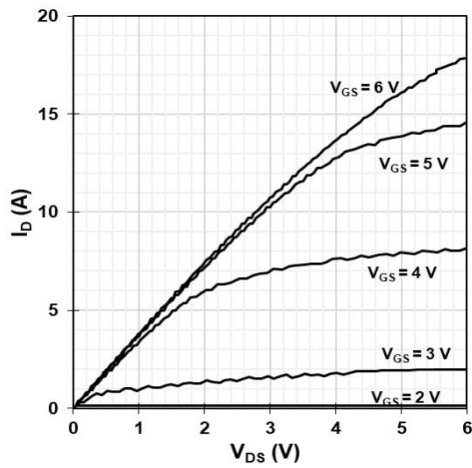
Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-drain reverse voltage	V_{SD}	-	4	-	V	$V_{GS} = 0 \text{ V}; I_{SD} = 2.2 \text{ A}$
Pulsed current, reverse	$I_{S, \text{pulse}}$	-	-	10	A	$V_{GS} = 6 \text{ V}$
Reverse recovery charge ¹	Q_{rr}	-	0	-	nC	$I_{SD} = 2.2 \text{ A}; V_{DS} = 400 \text{ V}$
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

1. Excluding Q_{OSS}

3 Electrical characteristics diagrams

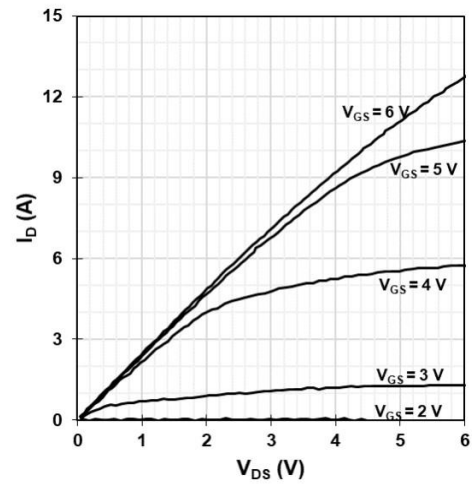
at $T_j = 25\text{ }^{\circ}\text{C}$, unless specified otherwise.

Figure 1 Typ. output characteristics



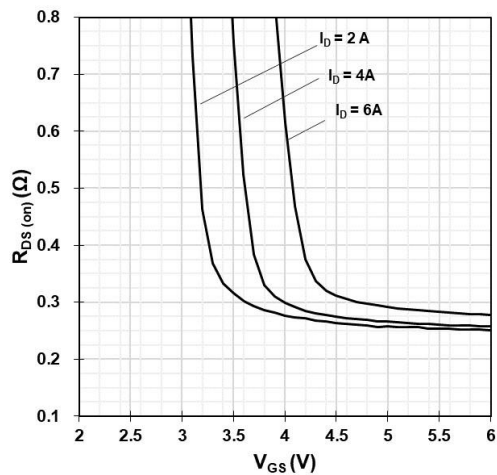
$$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^{\circ}\text{C}$$

Figure 2 Typ. output characteristics



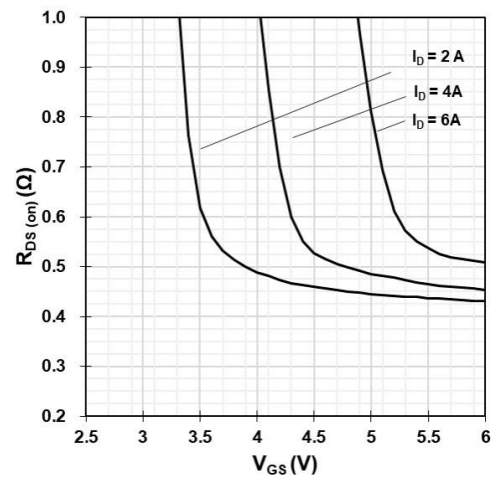
$$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ }^{\circ}\text{C}$$

Figure 3 Typ. drain-source on-state resistance

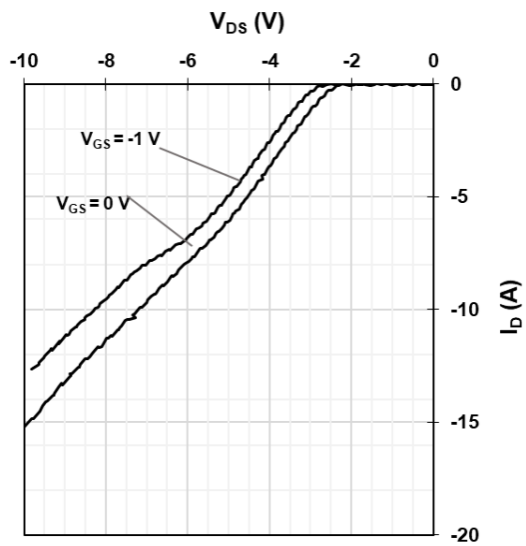


$$R_{DS(on)} = f(I_D, V_{GS}); T_j = 25\text{ }^{\circ}\text{C}$$

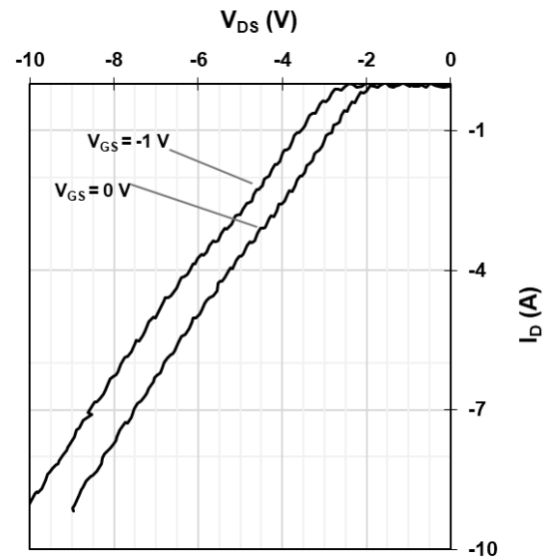
Figure 4 Typ. drain-source on-state resistance



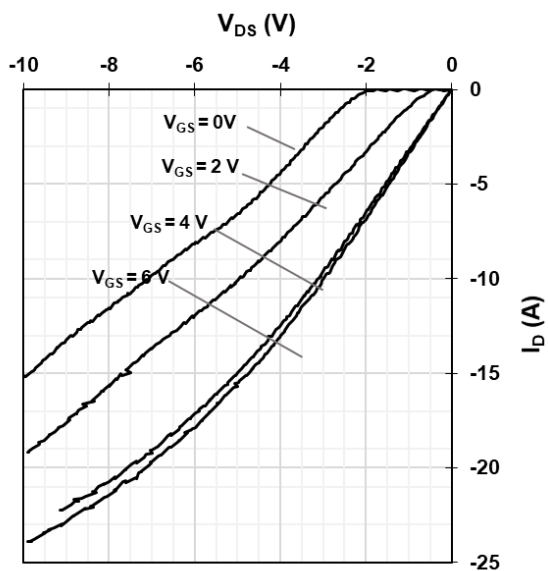
$$R_{DS(on)} = f(I_D, V_{GS}); T_j = 125\text{ }^{\circ}\text{C}$$

Figure 5 Typ. channel reverse characteristics


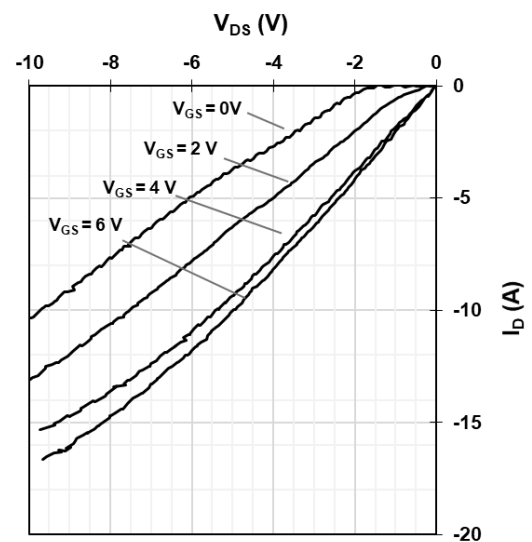
$$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^{\circ}\text{C}$$

Figure 6 Typ. channel reverse characteristics


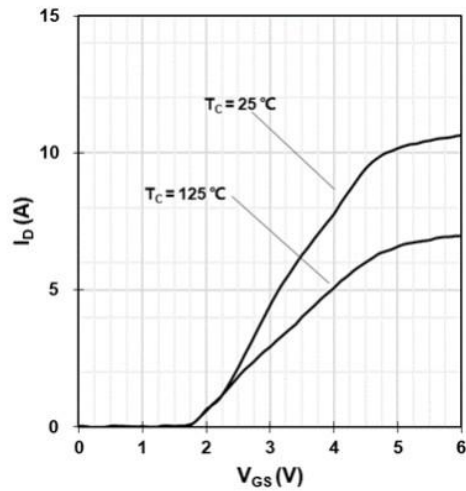
$$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ }^{\circ}\text{C}$$

Figure 7 Typ. channel reverse characteristics


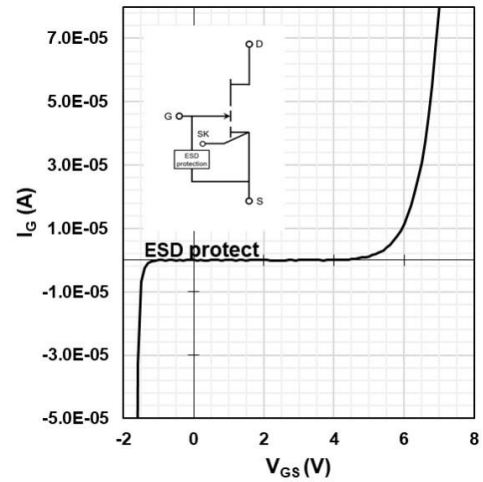
$$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^{\circ}\text{C}$$

Figure 8 Typ. channel reverse characteristics


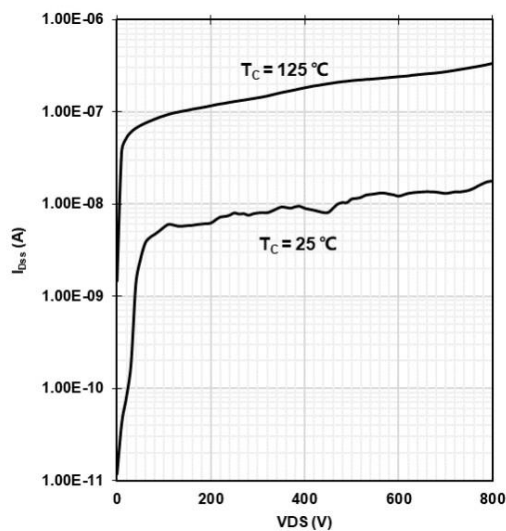
$$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ }^{\circ}\text{C}$$

Figure 9 Typ. transfer characteristics


$$I_D = f(V_{GS}); V_{DS} = 3 \text{ V}$$

Figure 10 Typ. gate-to-source leakage


$$I_G = f(V_{GS}); V_D = \text{open}$$

Figure 11 Drain-source leakage characteristics


$$I_{DSS} = f(V_{DS}); V_{GS} = 0 \text{ V}$$

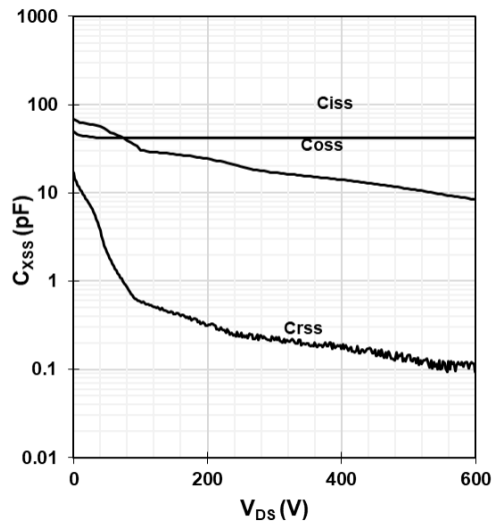
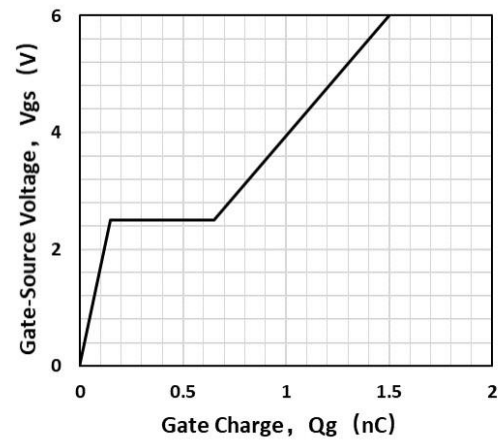
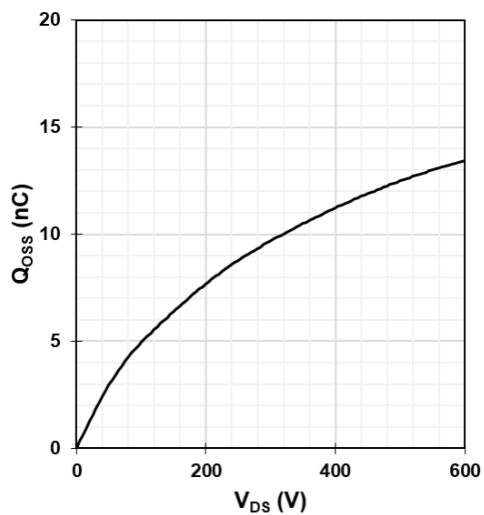
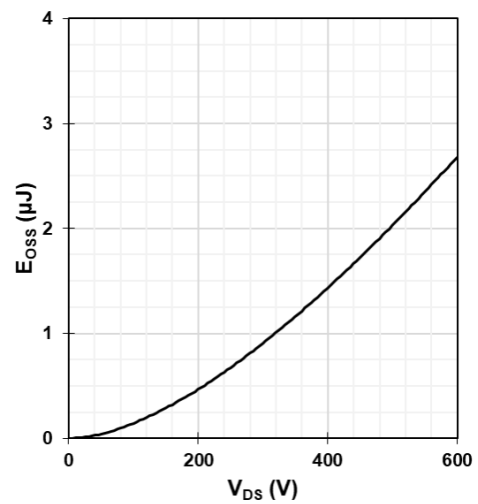
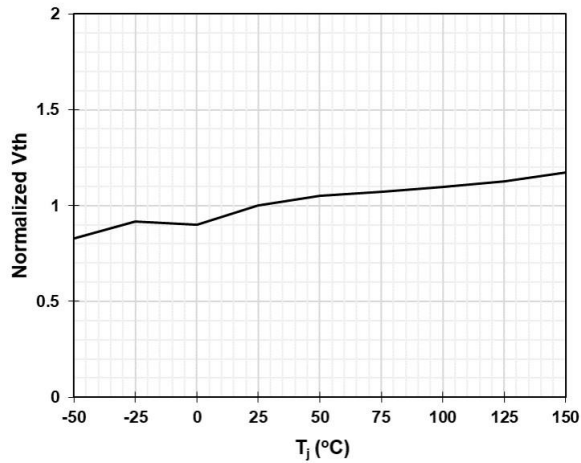
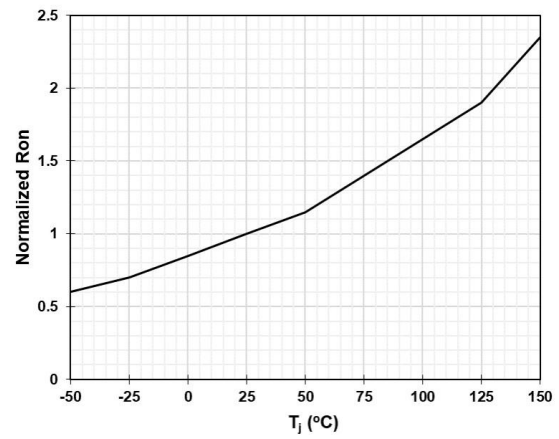
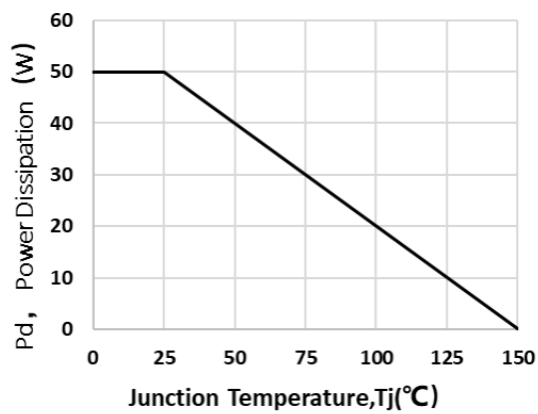
Figure 12 Typ. capacitances

 $C_{XSS} = f(V_{DS}); \text{Freq.} = 100\text{kHz}$
Figure 13 Typ. gate charge

 $V_{GS} = f(Q_G); V_{DS} = 400\text{ V}; I_D = 2.2\text{ A}$
Figure 14 Typ. output charge

 $Q_{OSS} = f(V_{DS}); \text{Freq.} = 100\text{kHz}$
Figure 15 Typ. C_{OSS} stored energy

 $E_{OSS} = f(V_{DS}); \text{Freq.} = 100\text{kHz}$

Figure 16 Gate threshold voltage


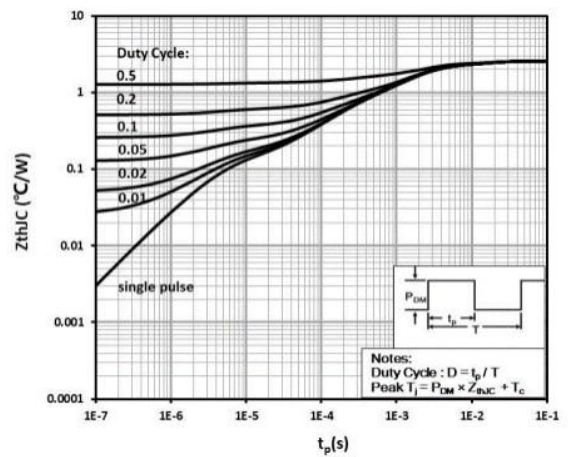
$$V_{GS(TH)} = f(T_j); V_{GS} = V_{DS}; I_D = 6 \text{ mA}$$

Figure 17 Drain-source on-state resistance


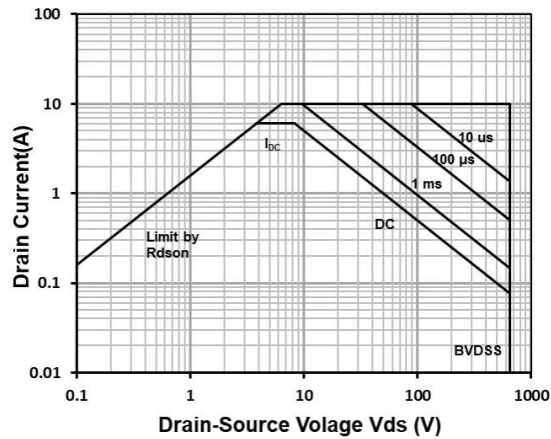
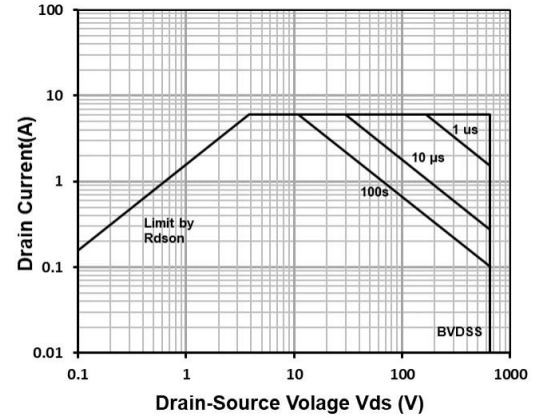
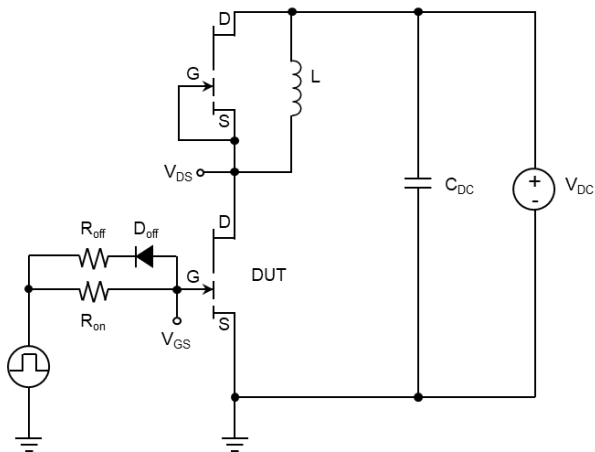
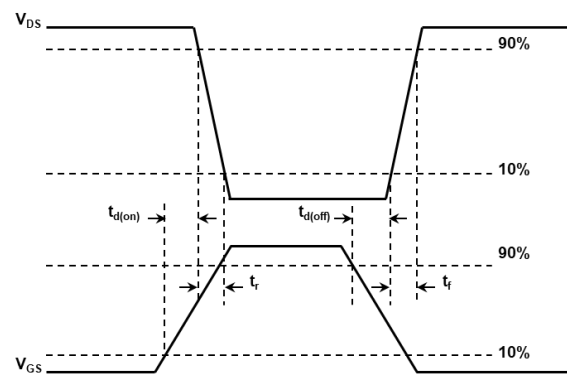
$$R_{DS(on)} = f(T_j); I_D = 2.2 \text{ A}; V_{GS} = 6 \text{ V}$$

Figure 18 Power dissipation


$$P_{tot} = f(T_c)$$

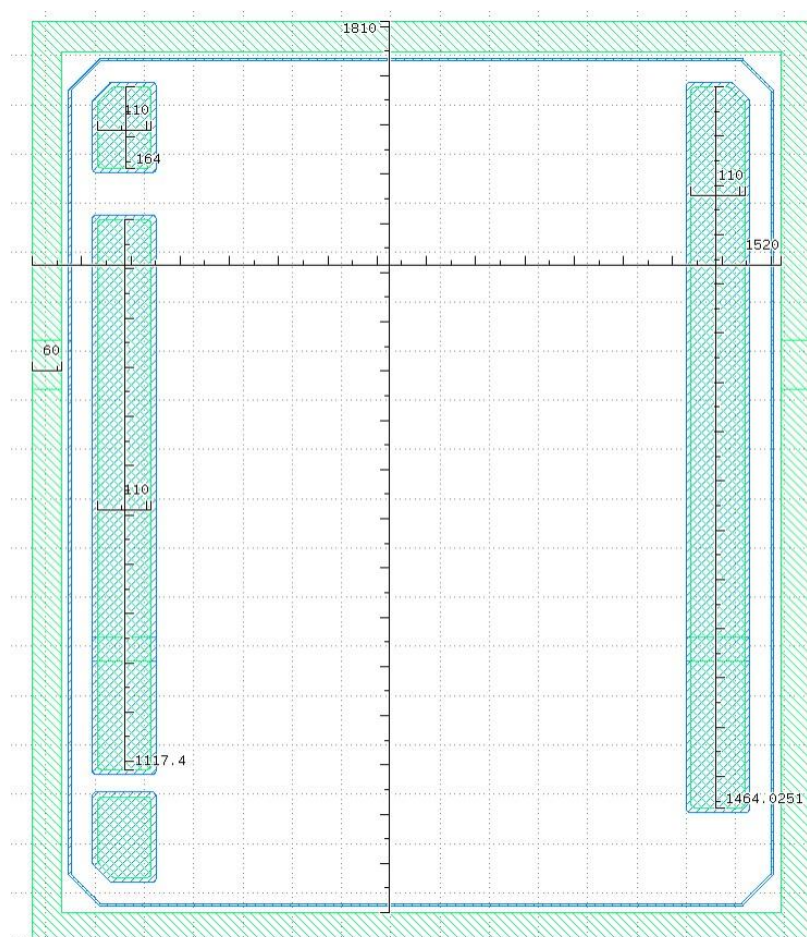
Figure 19 Max.transient thermal impedance


$$Z_{thjc} = f(t_p, D)$$

Figure 20 Safe Operation Area

 $I_d = f(V_{ds}); T_c = 25^\circ\text{C}$
Figure 21 Safe Operation Area

 $I_d = f(V_{ds}); T_c = 125^\circ\text{C}$
Figure 22 Switching time test circuit

 $V_{DS} = 400\text{ V}, I_D = 4.4\text{ A}, L = 318\text{ }\mu\text{H}, V_{GS} = 6\text{ V},$
Figure 23 Typ. switching time waveforms

 $R_{on} = 10\text{ }\Omega, R_{off} = 2\text{ }\Omega$

4 Chip Information

Parameter	
Wafer Size	6inch
Die size (With SL)	1810um*1520um
Gate Pad Size	164um*110um
Source Pad Size	1117um*110um
Drain Pad Size	1520um*110um
Scribe Line Size (PI CD)	60um
Top metal	4um, AlSi
Chip surface	3 um SiO ₂ + 0.5um SiN+10um PI
Recommended dicing method	Direct cutting without laser grooving



5 Wafer Information

基本资料设定
 * Wafer Size
 6 寸

Technology ID
 D65PX11

Product ID
 AC0030A1

Query

* Shot Size
 Width 19.91 mm
 Height 19.76 mm

* Shot Die数量
 * X Die 11 颗
 * Y Die 13 颗

Die Size
 X Die 1.810000 mm
 Y Die 1.520000 mm

Query

PCM修改

* 外型设定
 * 缩进量 10 mm

* 圆心位移
 * 横向 0 μm
 * 纵向 0 μm

平边位置
 * 大边 度
 小边 度

预览

平边尺寸
 * 大边 mm
 小边 mm

Notch位置
 * 0 度

预览

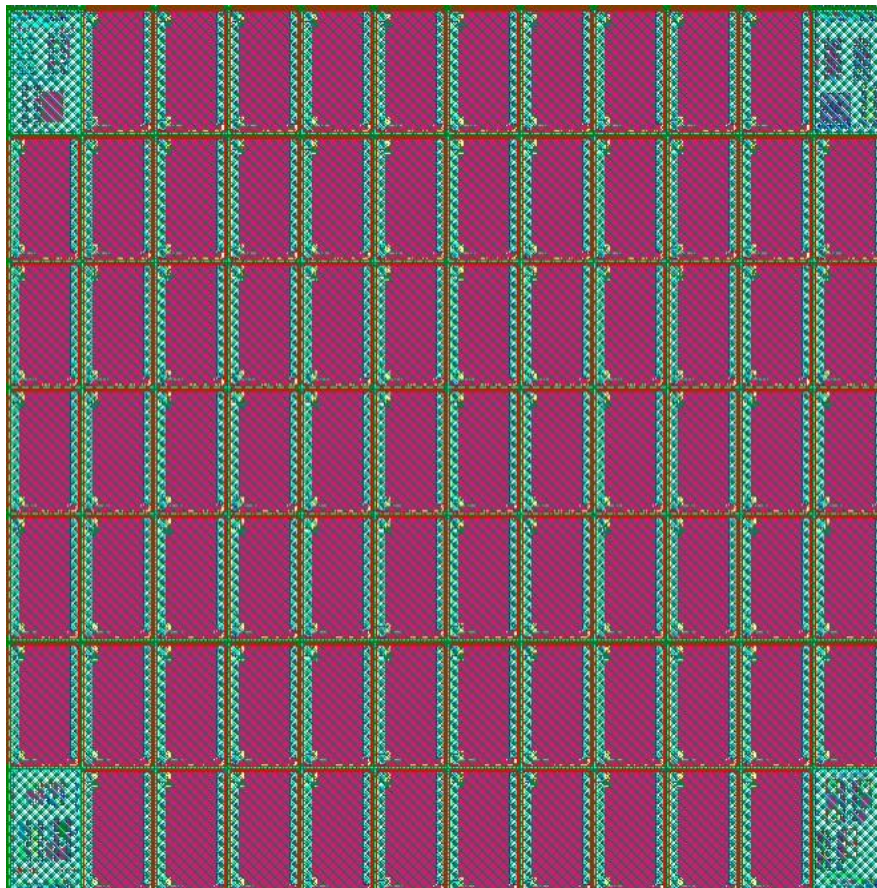
绘图结果

Gross Die数量:	4483	Die Pitch_X(μm):	1810.0	Die Pitch_Y(μm):	1520.0
PCM In Die:	192	Complete Shot:	21	Partial Shot:	24

导出

导出Map

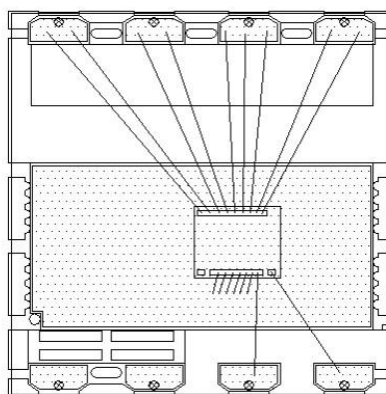
保存



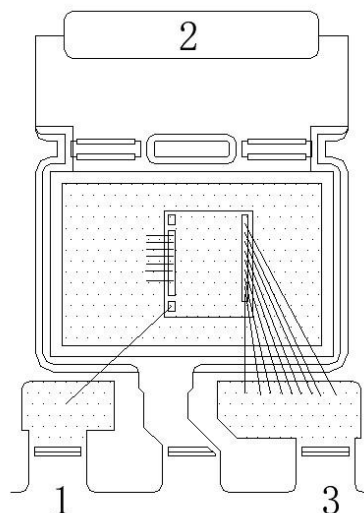
6 Bonding Information

Recommended wire	Cu Wire
Recommended wire diameter	1mil to 1.5mil
Recommended Package	DFN8*8, TO252, DFN5*6

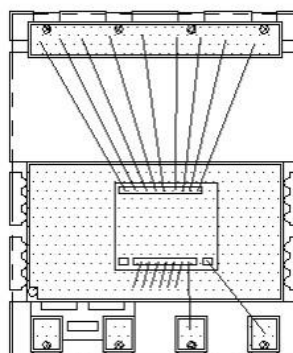
PKG	DFN8*8
Pad	1.5mils Cu Wires
Gate	1
Source	6
Drain	9
SK	1



PKG	TO252
Pad	1.5mils Cu Wires
Gate	1
Source	7
Drain	9



PKG	DFN5*6
Pad	1.5mils Cu Wires
Gate	1
Source	6
Drain	9
SK	1



7 Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2025-10-23	1.0 version release