Gallium Nitride E-Mode HEMT
GS700EDA360A: 360mΩ, 700V

Description

This is a 700V GaN-on-Si enhancement-mode power transistor in DFN5x6 package. The properties of GaN allow for high current, high breakdown voltage and high switching frequency. The DFN8x8 package offers low parasitic inductance, strong heat dissipation capability and high solderability, which make GaN apply better to consumer and industrial applications.

Features

- Ultra-low FOM
- Ultra-high switching frequency
- Reverse current capability
- Zero reverse recovery loss
- Monolithic integrated ESD protection
- RoHS, Pb-free, REACH-compliant

Applications

- AC/DC converters
- DC/DC converters
- Bridgeless totem pole PFC
- Fast chargers
- Power adapters
- LED lighting drivers
- Wireless power transfer
- Laser drivers
- TV display

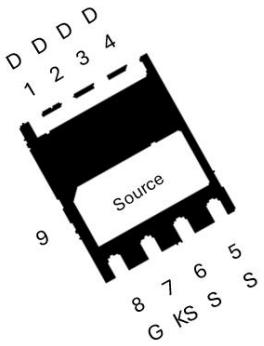


Table 1 Key Performance Parameters at T_j = 25 °C

Parameters	Values	Units
$V_{DS,\ max}$	700	V
$R_{DS(on),\ max}$	500	mΩ
Q_G	1.4	nC
$I_{D,\ Pulse}$	9	A
Q_{OSS} @ 400 V	8.9	nC

Table 2 Pin Information

Gate	Drain	Kelvin Source	Source
8	1,2,3,4	7	5,6,9

Table 3 Ordering Information

Ordering Code	Package	Product code	MOQ
GS700EWF360G0	DFN5x6	GS700EDA360A	3wk/reel

Table of contents

1 Maximum ratings

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime.

Table 3 Maximum rating

Parameters	Symbols	Values	Units	Notes/Test Conditions
Drain-source voltage	$V_{DS, max}$	700	V	V_{GS} = 0 V Tj = -55℃ to 150℃
Drain-source voltage transient [1]	$V_{DS, transient}$	800	V	V_{GS} = 0 V
Continuous current, drain-source	I_D	5	A	T_c = 25 °C
Pulsed current, drain-source [2]	$I_{D, pulse}$	9	A	T_c = 25 °C; V_G = 6 V
Pulsed current, drain-source [2]	$I_{D, pulse}$	4	A	T_c = 125 °C; V_G = 6 V
Gate-source voltage, continuous	V_{GS}	-1 to +7	V	T_j = -55 °C to 150 °C
Gate-source voltage, pulsed	$V_{GS, pulse}$	-20 to +10	V	T_j = -55 °C to 150 °C; t_{Pulse} = 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	40	W	T_c = 25 °C
Operating temperature	T_j	-55 to +150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 µs.
2. Pulse width = 10 µs.

2 Thermal characteristics

Table 4 Thermal characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-ambient	R_{thJA}		80		°C/W	
Thermal resistance, junction-case	R_{thJC}	-	3.2	-	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

3 Electrical characteristics

at T_j = 25 °C, unless specified otherwise.

Table 5 Static characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.2	1.6	2.5	V	I_D = 4mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	2	-		I_D = 4 mA; V_{DS} = V_{GS}; T_j = 150 °C
Drain-source leakage current	I_{DSS}	-	0.01	0.5	μA	V_{DS} = 700 V; V_{GS} = 0 V; T_j = 25 °C
		-	3	-		V_{DS} = 700 V; V_{GS} = 0 V; T_j = 150 °C
Gate-source leakage current	I_{GSS}	-	0.7		μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	360	500	mΩ	V_{GS} = 6 V; I_D = 2 A; T_j = 25 °C
		-	940	-	mΩ	V_{GS} = 6 V; I_D = 2 A; T_j = 150 °C
Gate resistance	R_G	-	13.5	-	Ω	f = 5 MHz; open drain

Table 6 Dynamic characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	37	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100KHz
Output capacitance	C_{oss}	-	13	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100KHz
Reverse transfer capacitance	C_{rss}	-	0.01	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100KHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	16	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	28	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	8.9	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Turn-on delay time	$t_{d(on)}$	-	3	-	ns	V_{DS} = 400 V; I_D = 4 A; L = 318 μH; V_{GS} = 6 V; R_{on} = 10 Ω; R_{off} = 2 Ω
Turn-off delay time	$t_{d(off)}$	-	6	-	ns	
Rise time	t_r	-	5	-	ns	
Fall time	t_f	-	9	-	ns	

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

Table 7 Gate charge characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	Q_G	-	1.4	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D = 2 A
Gate-source charge	Q_{GS}	-	0.3	-	nC	
Gate-drain charge	Q_{GD}	-	0.8	-	nC	
Gate plateau voltage	V_{plat}	-	2.5	-	V	V_{DS} = 400 V; I_D = 2 A

Table 8 Reverse conduction characteristics

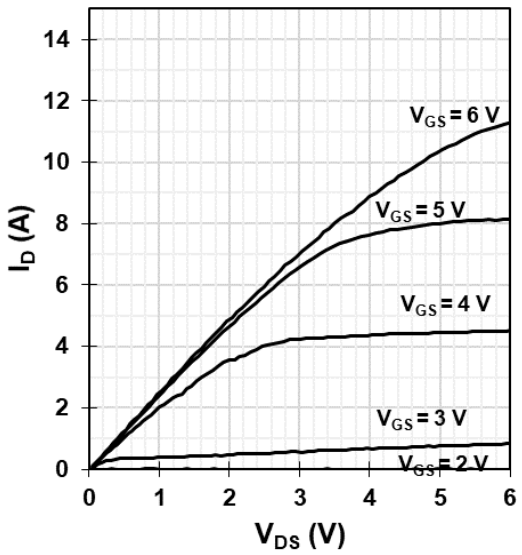
Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-drain reverse voltage	V_{SD}	-	4.4	-	V	V_{GS} = 0 V; I_{SD} = 2 A
Pulsed current, reverse	$I_{S,\ pulse}$	-	-	9	A	V_{GS} = 6 V
Reverse recovery charge [1]	Q_{rr}	-	0	-	nC	I_{SD} = 2 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

1. Excluding Q_{OSS}

4 Electrical characteristics diagrams

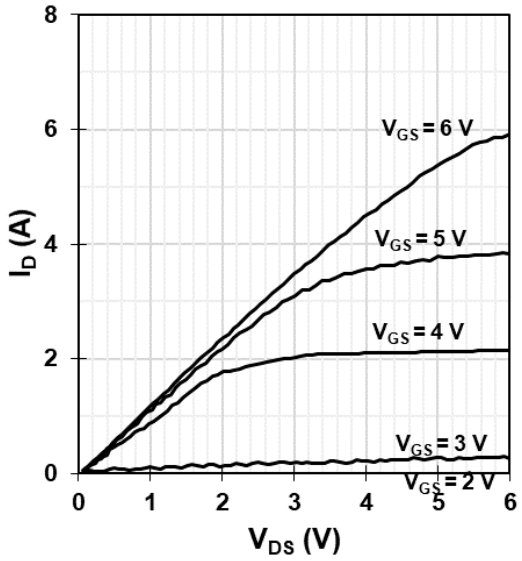
at T_j = 25 °C, unless specified otherwise.

Figure 1 Typ. output characteristics



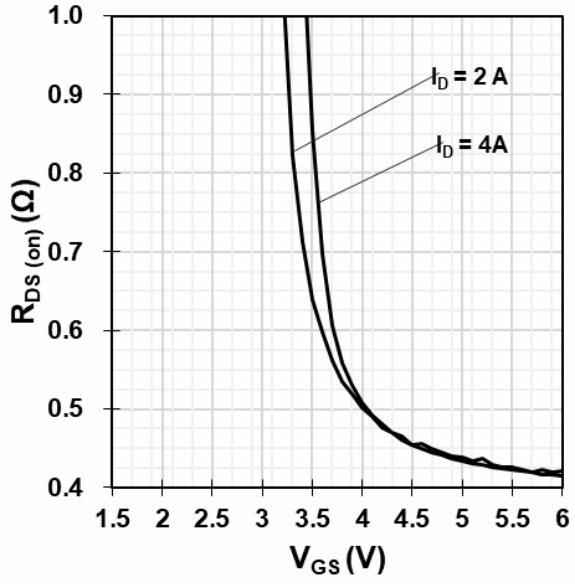
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



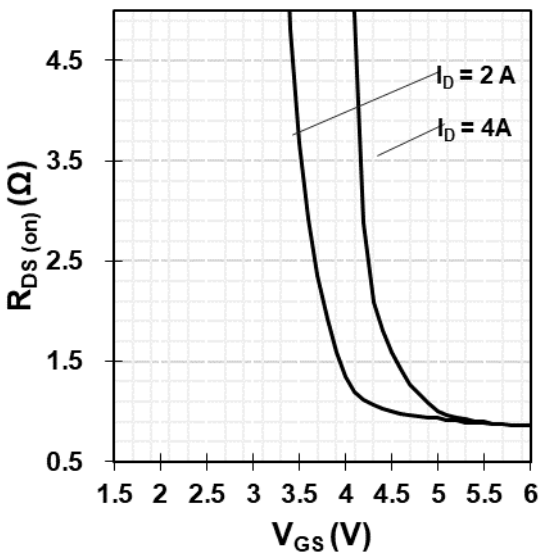
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 3 Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 25 °C

Figure 4 Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 125 °C

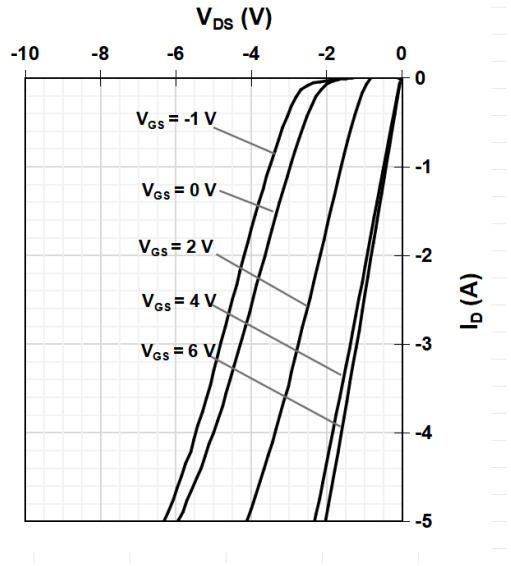
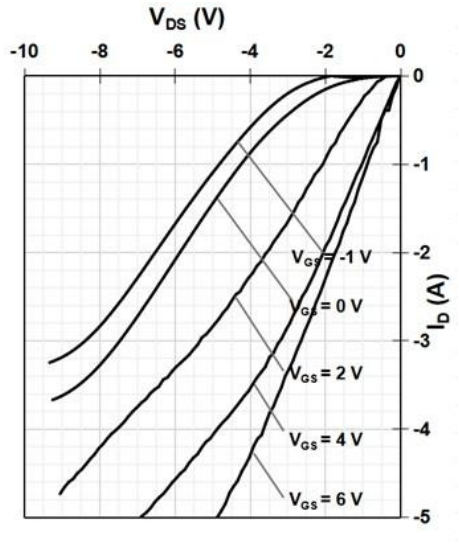
Figure 5 Typ. channel reverse characteristics	Figure 6 Typ. channel reverse characteristics
	
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 ℃	$I_D = f(V_{DS}, V_{GS})$; T_j = 125 ℃

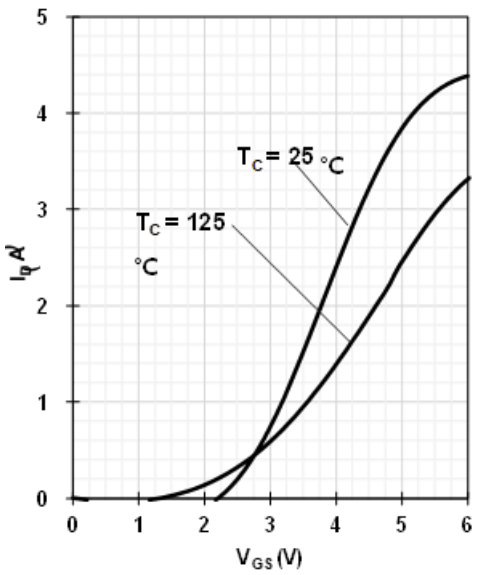
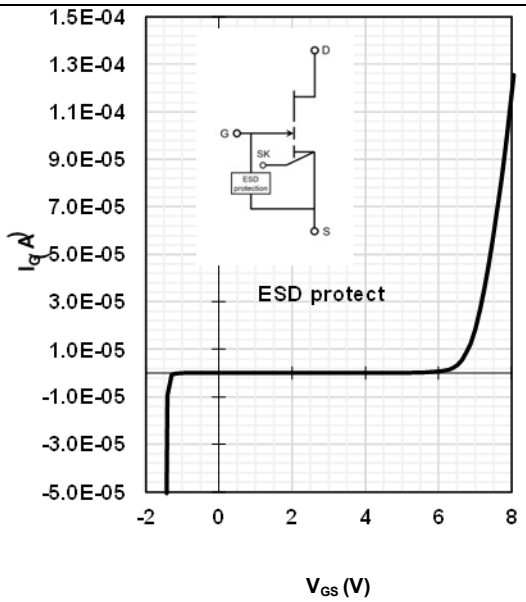
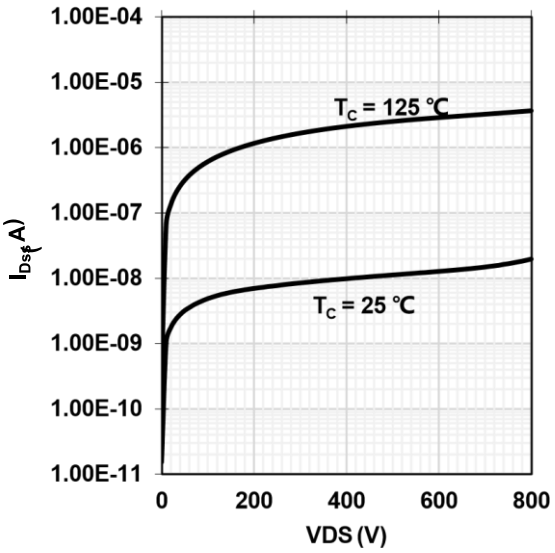
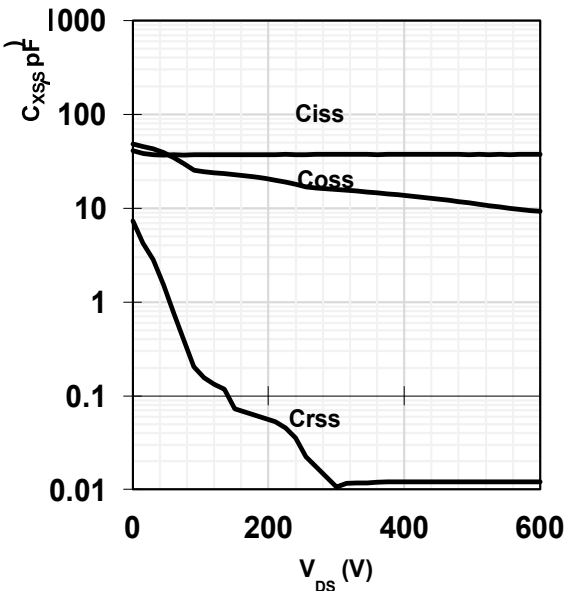
Figure 7 Typ. transfer characteristics	Figure 8 Typ. gate-to-source leakage
	
$I_D = f(V_{GS})$; V_{DS} = 3 V	$I_G = f(V_{GS})$; V_D = open

Figure 9 Drain-source leakage characteristics



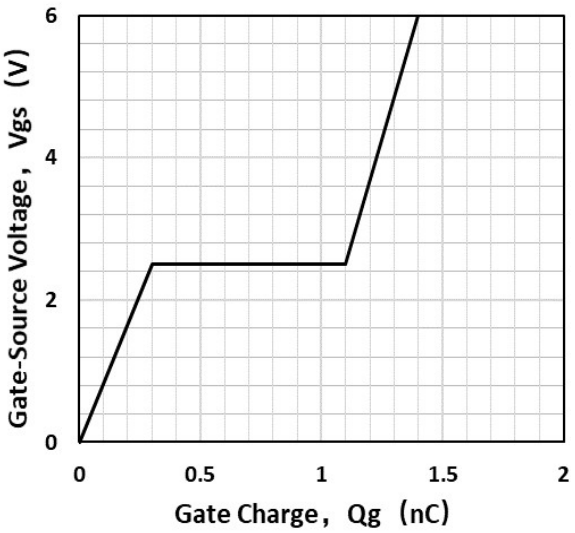
Idss = f(Vds); Vgs = 0V

Figure 10 Typ. capacitances



C_{XSS} = f(V_{DS}); Freq. = 100kHz

Figure 11 Typ. gate charge



V_{GS} = f(Q_G); V_{DS} = 400 V; I_D = 2 A

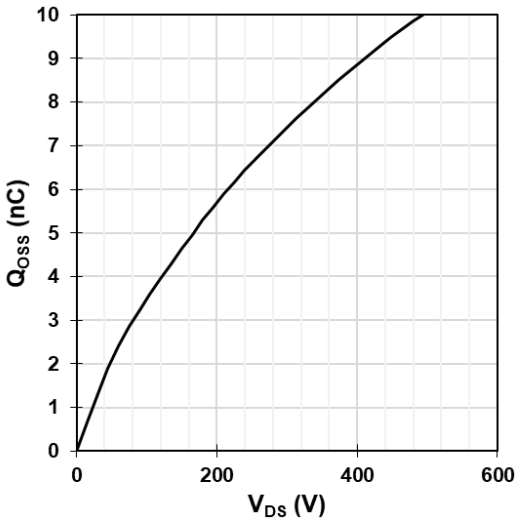
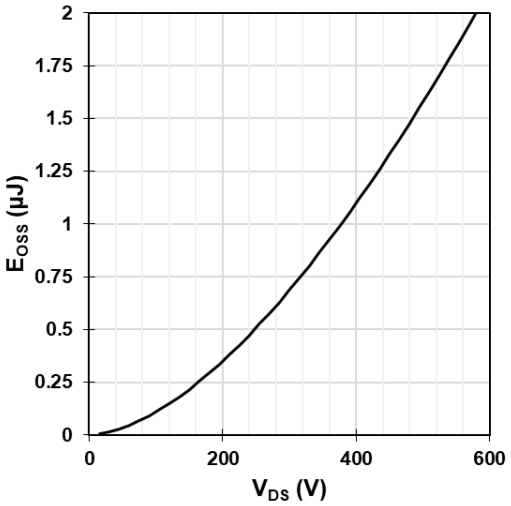
Figure 12 Typ. output charge	Figure 13 Typ. C_{oss} stored energy
	
Q_{OSS} = f(V_{DS}); Freq. = 100khz	E_{OSS} = f(V_{DS}); Freq. = 100khz

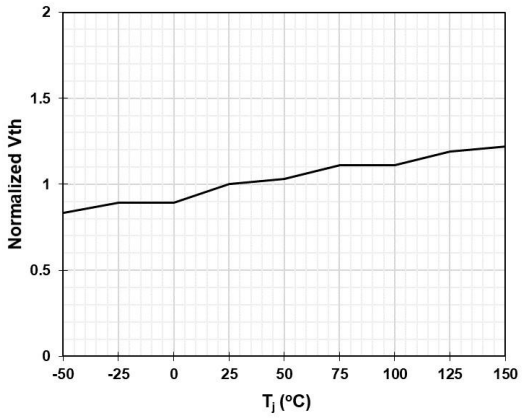
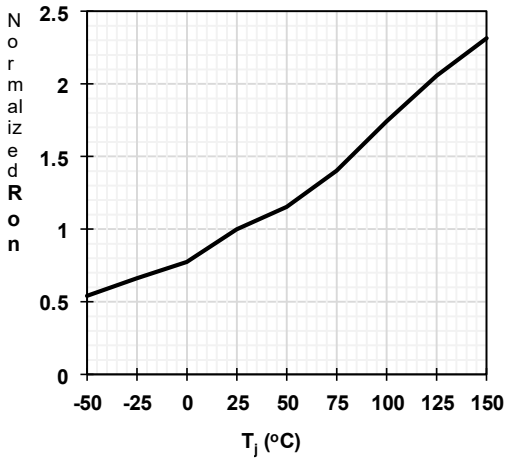
Figure 14 Gate threshold voltage	Figure 15 Drain-source on-state resistance
	
$V_{GS(TH)}$ = f(T_j); V_{GS} = V_{DS}; I_D = 16 mA	$R_{DS(on)}$ = f(T_j); I_D = 5 A; V_{GS} = 6 V

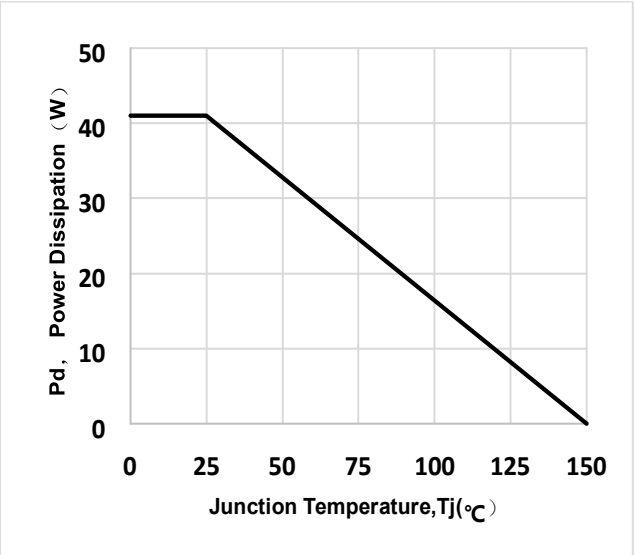
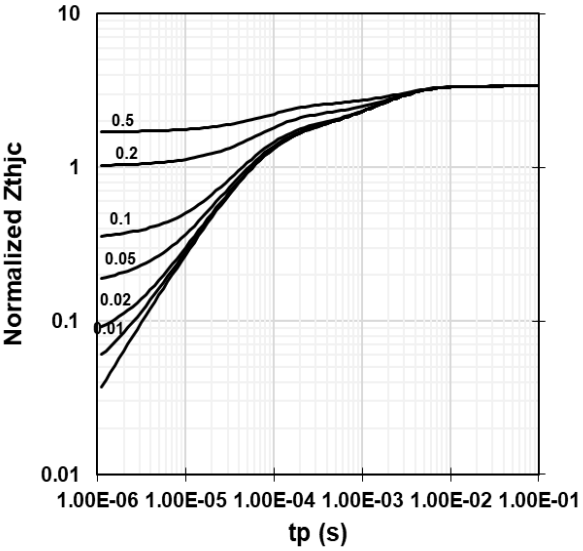
Figure 16 Power dissipation	Figure 17 Max.transient thermal impedance
	
Ptot = f(Tc)	Zthjc = f(tp,D)

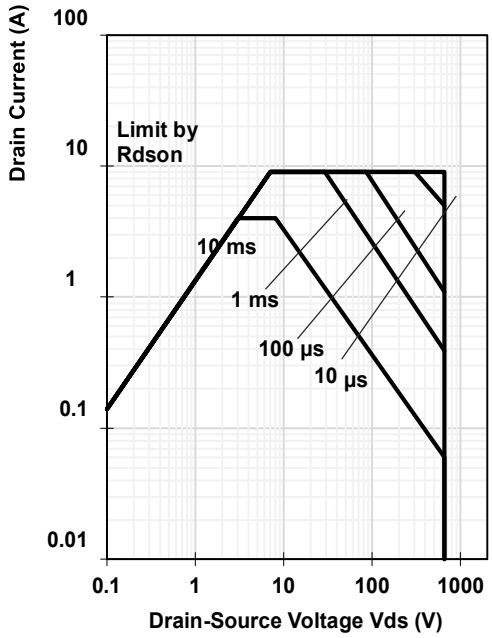
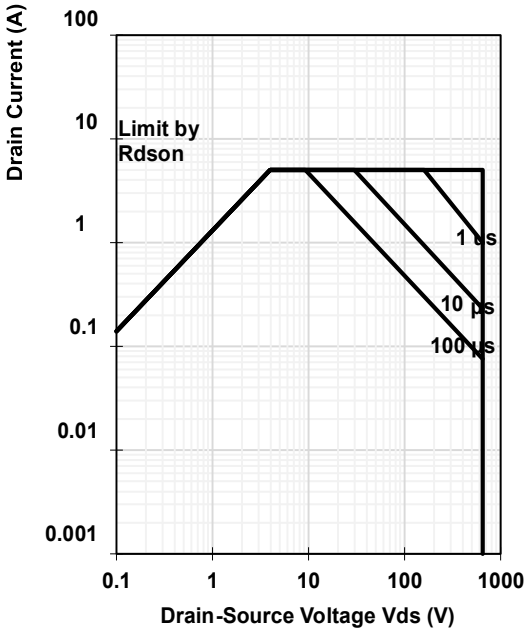
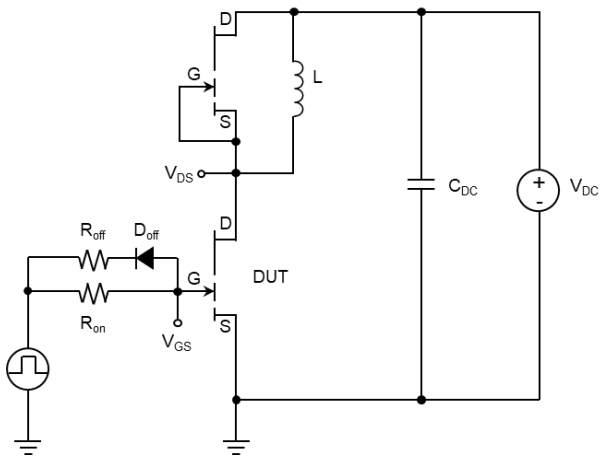
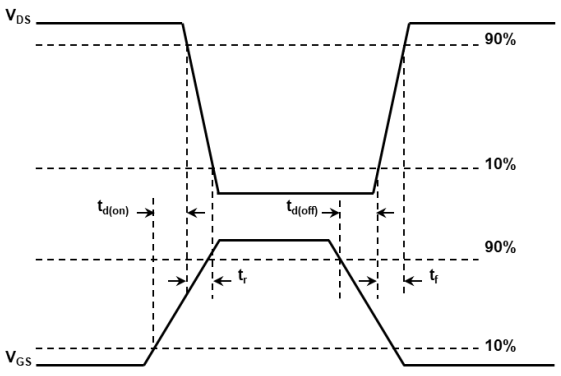
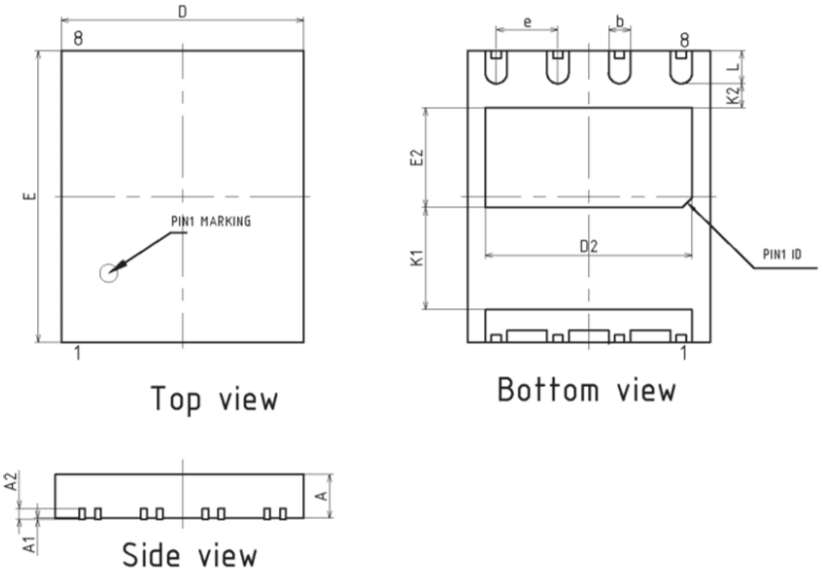
Figure 18 Safe Operation Area	Figure 19 Safe Operation Area
	
Id = f(Vds); Tc = 25℃	Id = f(Vds); Tc = 125℃

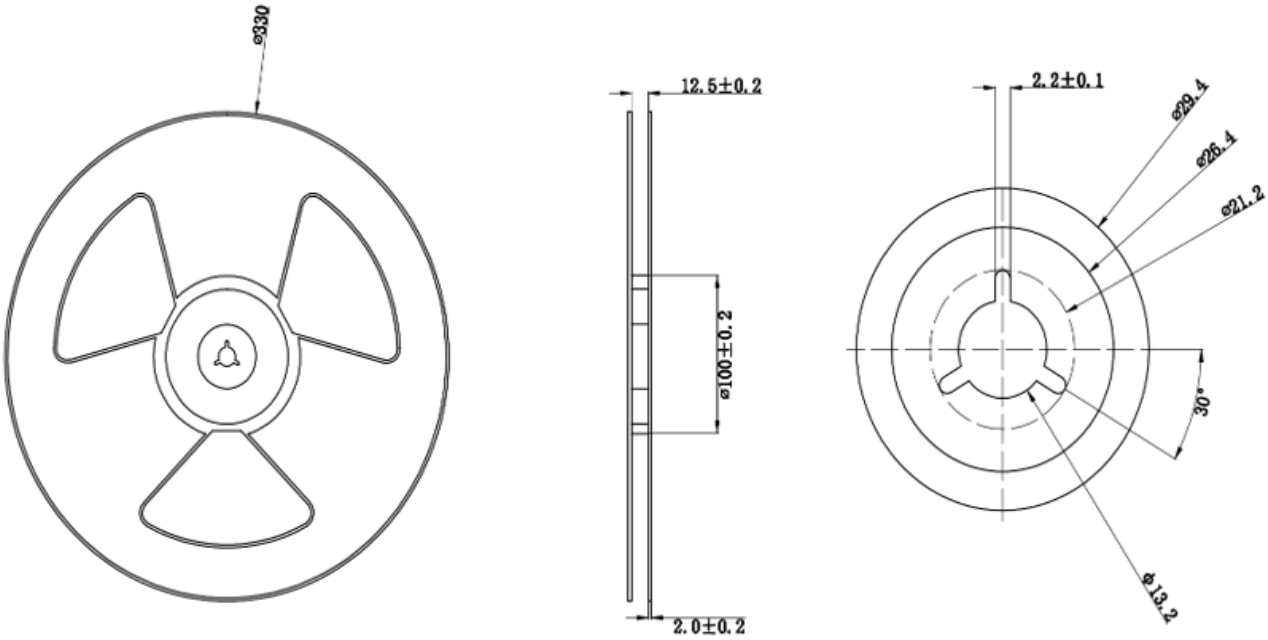
Figure 20 Switching time test circuit	Figure 21 Typ. switching time waveforms
	
V_{DS} = 400 V, I_D = 6 A, L = 318 μH, V_{GS} = 6 V, R_{on} = 10 Ω, R_{off} = 2 Ω	

5 Package outlines



SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.203REF	
b	0.40	0.45	0.50
D	4.90	5.00	5.10
D2	4.16	4.26	4.36
e		1.27	
E	5.90	6.00	6.10
E2	1.95	2.05	2.15
L	0.575	0.675	0.775
K1		2.10REF	
K2		0.50REF	

6 Reel Information



7 Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2025-01-23	1.0 version release
2.0	2025-04-25	Updated Electrical Cz Data and Diagram and Implemented the Reel Information