Gallium Nitride E-mode HEMT
GS650EDC1K0A: 1000 mΩ, 650V

Description

Gallium Nitride High-Electron-Mobility Transistors (HEMTs) have shown outstanding results in high power applications. The large bandgap results in a high breakdown field, allowing for high operating voltages. Its inherent two-dimensional electron gas (2-DEG) at the AlGaN/GaN interface yields a high electron sheet charge density and mobility, significantly reducing resistive losses in power transistors. Additionally, due to the low gate charge and reverse recovery charge, the switching losses are reduced and switching speeds increased compared to traditional silicon power devices. The p-GaN gate is implemented to ensure the desired enhancement mode (normally-off) operation and improved slew rates.

The GS650EDC1K0A can be delivered as separate dice in waffle pack or packaged in a DFN 8x8 or DFN 5x6 with exposed paddle allowing an excellent thermal contact.

Features

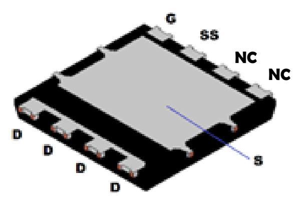
- 650V enhancement mode power transistor
- 850V transient drain-to-source voltage
- RDS,ON = 1000 mΩ
- IDS,MAX = 1,6 A
- Ultra-low FOM
- Simple gate drive requirements: 0 to 6 V
- Transient tolerant gate drive: -20 V / +10 V
- High switching frequency > 1 MHz
- Reverse conduction capability
- Zero reverse recovery loss

Applications

- Wall wart adapters
- Power Factor Correction
- LED drivers
- Battery Chargers
- Industrial Power Supplies
- Motor drivers

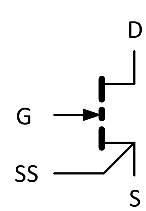
Outline

Package



Die

Symbol



Ordering

The GS650EDC1K0A is not a product for sale. It is a product sample to demonstrate the capabilities of the Power GaN process.

Absolute Maximum Ratings (T_J = 25°C unless otherwise noted)

Table 1

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Drain to Source Voltage	V_{DS}	650	V
Drain to Source Voltage – transient (note 1)	$V_{DS,trans}$	850	V
Gate to Source Voltage	V_{GS}	-10 to +7	V
Gate to Source Voltage – transient (note 1)	$V_{GS,trans}$	-20 to + 10	V
Drain Current – continue	I_{DS}	1,6	A
Pulsed Drain Current (note 2)	$I_{DS,P}$	2,7	A

(1) For t ≤ 1 µs
(2) Pulse width 10 µs, V_{GS} = 6 V

Thermal Characteristics QFN 8x8 (Typical Values unless otherwise noted)

Table 2

Parameter	Symbol	Value	Unit
Thermal Resistance Junction – to – Case	$R_{\Theta\text{-}JC}$	1,4	K/W
Thermal Resistance Junction – to – Ambient (3)	$R_{\Theta\text{-}JA}$	36,5	K/W
Maximum Solder Temperature	T_{SOLD}	260	°C

(3) JEDEC JESD51

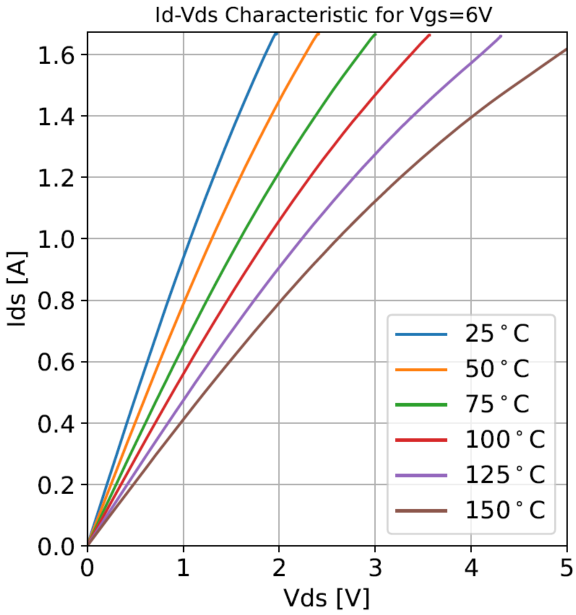
Electrical Characteristics (Typical Values @ T_J = 25°C unless otherwise noted)

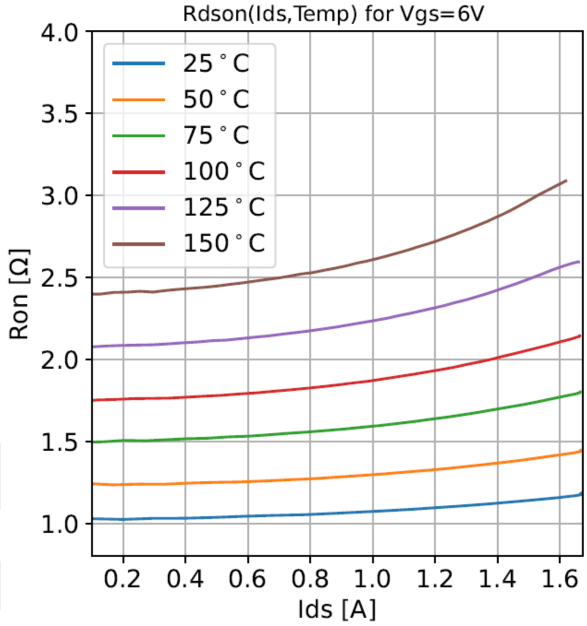
Table 3

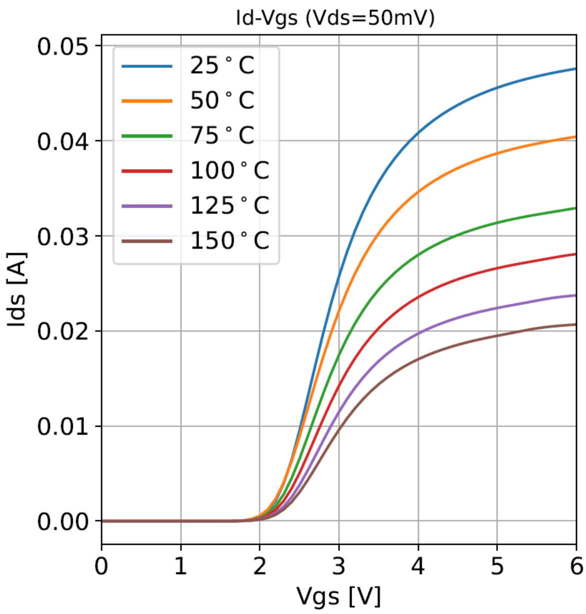
Parameter	Condition	Symbol	Min	Typ	Max	Unit
Drain to Source Blocking Voltage	V_{GS} = 0 V, I_{DSS} ≤ 18 µA	V_{BDSS}	650			V
On Resistance	V_{GS} = 6 V, I_{DS} = 1 A	R_{DSon}		1000	1300	mΩ
Gate Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 0,3 mA	V_{Th}	0.9	2.0	3.0	V
Gate to Source Current	V_{GS} = 6 V, V_{DS} = 0 V	I_{GS}		45		µA
Drain to Source Leakage Current	V_{DSS} = 650 V, V_{GS} = 0 V	I_{DSS}		0,10		µA
Input Capacitance	V_{DS} = 400 V V_{GS} = 0 V f = 100 kHz	C_{ISS}		11,5		pF
Output Capacitance		C_{OSS}		5,9		pF
Reverse Transfer Capacitance		C_{RSS}		0,01		pF
Output Charge	V_{DS} = 400 V, V_{GS} = 0 V	Q_{OSS}		3,5		nC
Output Cap stored energy	V_{DS} = 400 V V_{GS} = 0 V, f = 100 kHz	E_{OSS}		0,6		µJ
Total Gate Charge	Vds = 0 to 400 V, Vgs = 0 to 6 V	Qg		0,3		nC
Effective Output Capacitance, Energy related	Vds = 0 to 400 V, Vgs = 0 V	$Co_{(er)}$		7,0		pF
Effective Output Capacitance, Time related	Vds = 0 to 400 V, Vgs = 0 V	$Co_{(tr)}$		8,7		pF

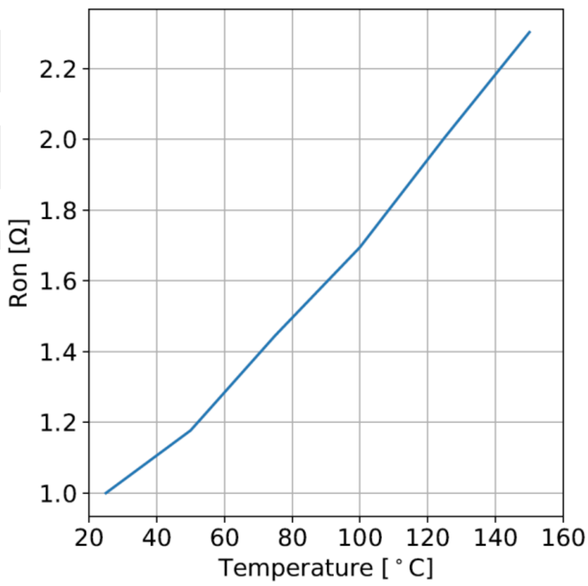
Note: Figures are based on a linear scaling of the 120 mΩ transistor

Electrical Graphs (1/2)

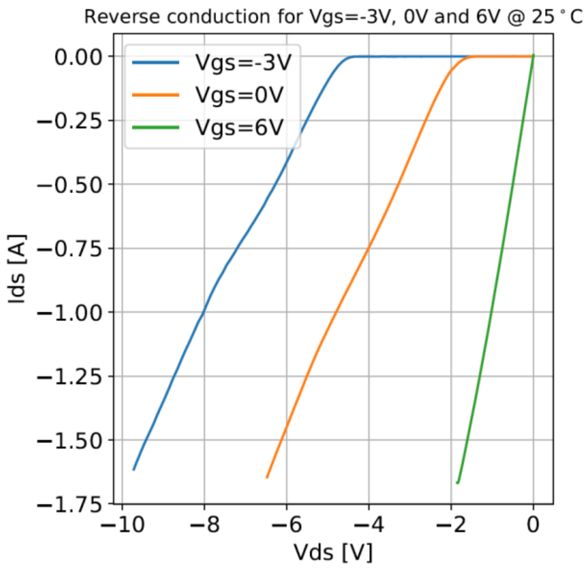


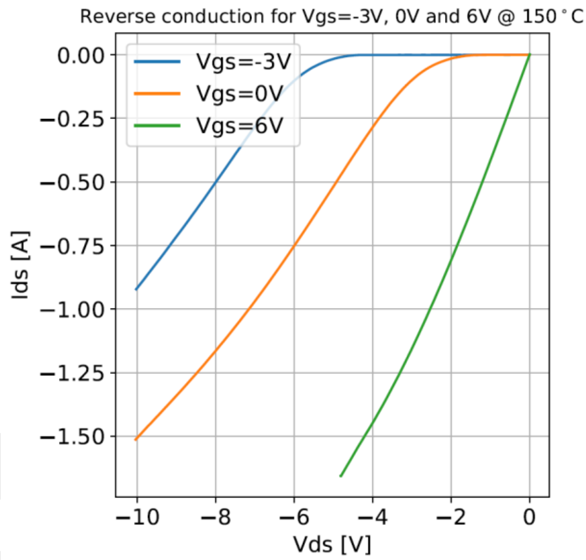


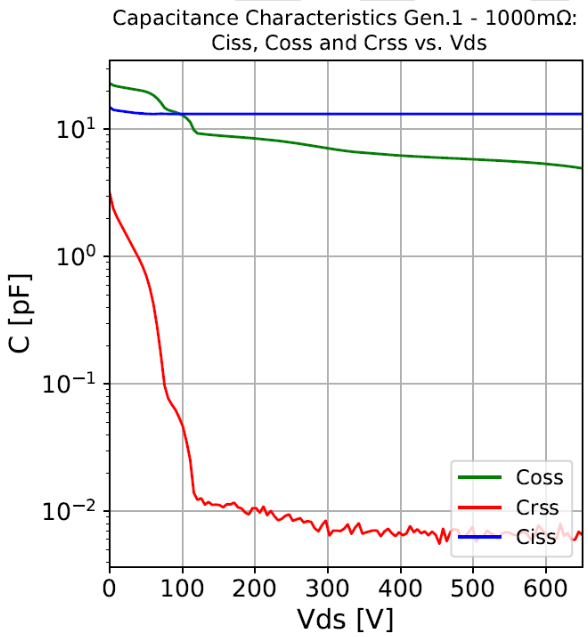


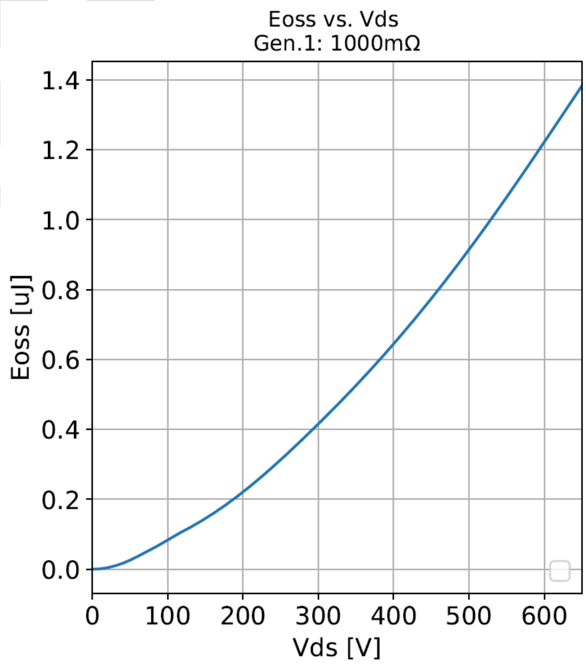


Electrical Graphs (2/2)









Test Circuits

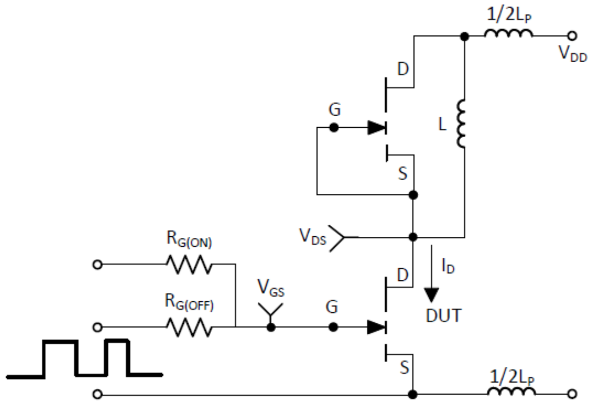


Fig 13: Switching Test Circuit

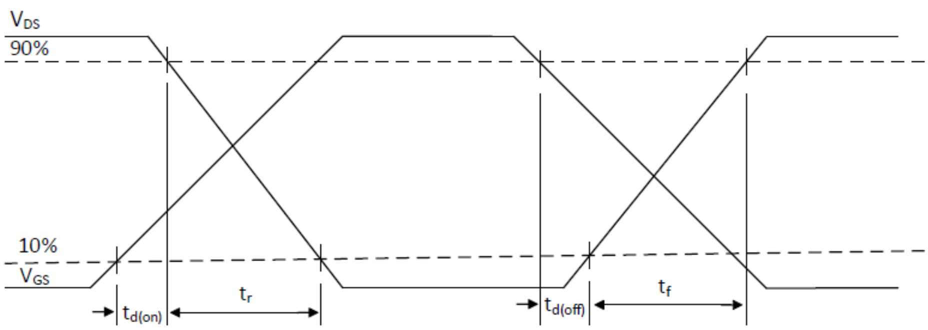
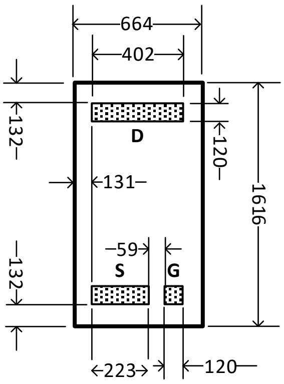


Fig 14: Switching Time Waveforms

Package Information

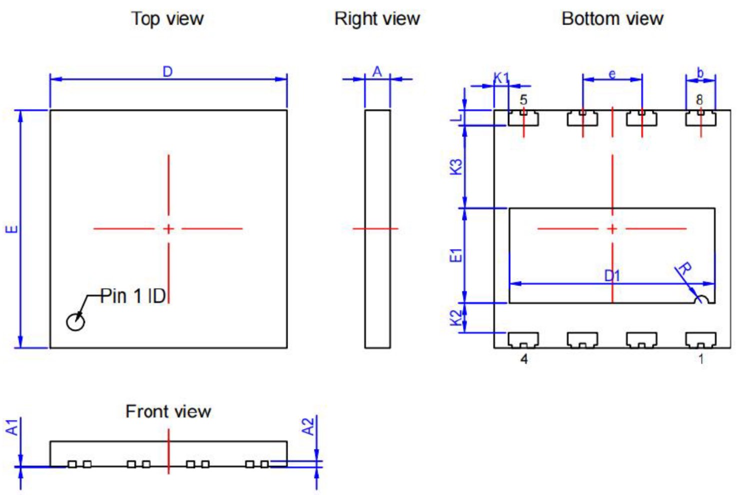
Bare Die

Dimensions of the pads in µm refer to the passivation and polyimide opening.
Drawing is not to scale.



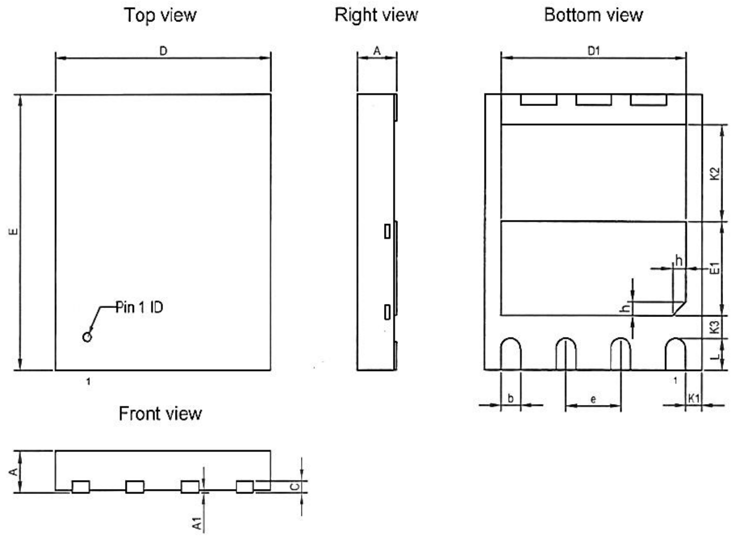
Marking

DFN 8x8



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.75	0.85	0.95
STAND OFF	A1	0.00	0.03	0.05
L/F THICKNESS	A2		0.203REF	
LEAD WIDTH	b	0.95	1.00	1.05
BODY SIZE X	D	7.90	8.00	8.10
EP SIZE X	D1	6.84	6.94	7.04
BODY SIZE Y	E	7.90	8.00	8.10
EP SIZE Y	E1	3.10	3.20	3.30
LEAD PITCH	e		2.00BSC	
SPACING	K1	0.40	0.50	0.60
SPACING	K2	0.90	1.00	1.10
SPACING	K3	2.70	2.80	2.90
LEAD LENGTH	L	0.40	0.50	0.60
RADIUS	R	0.15	0.25	0.35

DFN 5x6



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.80	0.85	0.90
STAND OFF	A1	0.00	0.02	0.05
L/F THICKNESS	A2		0.203REF	
LEAD WIDTH	b	0.40	0.45	0.50
BODY SIZE X	D	4.90	5.00	5.10
EP SIZE X	D1	4.16	4.26	4.36
BODY SIZE Y	E	5.90	6.00	6.10
EP SIZE Y	E1	1.95	2.05	2.15
LEAD PITCH	e		1.27BSC	
LEAD LENGTH	L	0.575	0.675	0.775
CHAMFER	h	0.20	0.30	0.40
GAP BETWEEN LEAD AND PKG	K1		0.27MIN	
GAP BETWEEN LEAD AND PAD	K2		2.00MIN	
GAP BETWEEN LEAD AND PAD	K3		0.40MIN	

Disclaimer

This Product Sample is not a finished product and is not available for sale to consumers. The Product Sample is only intended for research, development, demonstration, and evaluation purposes and will only be used in laboratory/development areas by persons with an engineering/technical training and familiar with the risks associated with handling electrical/mechanical components, systems and subsystems. These persons assume full responsibility/liability for proper and safe handling of the Product Sample. Any other use, resale or redistribution of the Product Sample for any other purpose is strictly prohibited.