

# Gallium Nitride E-mode HEMT

## GS650EDA470A: 470 mΩ, 650V

### Description

Gallium Nitride High-Electron-Mobility Transistors (HEMTs) have shown outstanding results in high power applications. The large bandgap results in a high breakdown field, allowing for high operating voltages. Its inherent two-dimensional electron gas (2-DEG) at the AlGaN/GaN interface yields a high electron sheet charge density and mobility, significantly reducing resistive losses in power transistors. Additionally, due to the low gate charge and reverse recovery charge, the switching losses are reduced and switching speeds increased compared to traditional silicon power devices. The p-GaN gate is implemented to ensure the desired enhancement mode (normally-off) operation and improved slew rates.

The GS650EDA470A can be delivered as separate dice in wafer pack or packaged in a DFN 8x8 or DFN 5x6 with exposed paddle allowing an excellent thermal contact

### Features

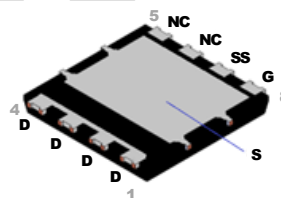
- 650V enhancement mode power transistor
- 850V transient drain-to-source voltage
- $R_{DS,ON} = 470 \text{ m}\Omega$
- $I_{DS,MAX} = 3,4 \text{ A}$
- Ultra-low FOM
- Simple gate drive requirements: 0 to 6 V
- Transient tolerant gate drive: -20 V / +10 V
- High switching frequency > 1 MHz
- Reverse conduction capability
- Zero reverse recovery loss

### Applications

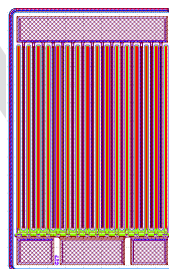
- Wall wart adapters
- Power Factor Correction
- LED drivers
- Battery Chargers
- Industrial Power Supplies
- Motor drivers

### Outline

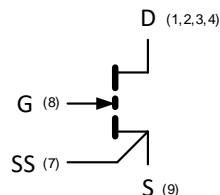
#### Package



#### Die



#### Symbol



### Ordering

The GS650EDA470A is not a product for sale. It is a product sample to demonstrate the capabilities of the Power GaN process.

**Absolute Maximum Ratings** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

**Table 1**

| Parameter                                    | Symbol         | Value       | Unit             |
|--|----------------|-------------|------------------|
| Operating Junction Temperature               | $T_J$          | -55 to +150 | $^\circ\text{C}$ |
| Drain to Source Voltage                      | $V_{DS}$       | 650         | V                |
| Drain to Source Voltage – transient (note 1) | $V_{DS,trans}$ | 850         | V                |
| Gate to Source Voltage                       | $V_{GS}$       | -10 to +7   | V                |
| Gate to Source Voltage – transient (note 1)  | $V_{GS,trans}$ | -20 to + 10 | V                |
| Drain Current – continue                     | $I_{DS}$       | 3,4         | A                |
| Pulsed Drain Current (note 2)                | $I_{DS,P}$     | 7,6         | A                |

(1) For  $t \leq 1 \mu\text{s}$

(2) Single Pulse,  $t_P = 10 \mu\text{s}$ ,  $V_{GS} = 6 \text{ V}$ ,  $R_{\theta-JC} = 1,4 \text{ K/W}$ ,  $Z_{\theta-JC} = 0,22$ ,  $T_J = 150^\circ\text{C}$ ,  $T_C = 125^\circ\text{C}$

$$I_{DS,P} = \sqrt{\frac{T_J - T_C}{R_{DSon(@T_J)} \times R_{\theta-JC} \times Z_{\theta-JC}}}$$

**Thermal Characteristics QFN 8x8** (Typical Values unless otherwise noted)

**Table 2**

| Parameter                                      | Symbol          | Value | Unit             |
|--|-----------------|-------|------------------|
| Thermal Resistance Junction – to – Case        | $R_{\theta-JC}$ | 1,4   | K/W              |
| Thermal Resistance Junction – to – Ambient (3) | $R_{\theta-JA}$ | 36,5  | K/W              |
| Maximum Solder Temperature                     | $T_{SOLD}$      | 260   | $^\circ\text{C}$ |

(3) JEDEC JESD51

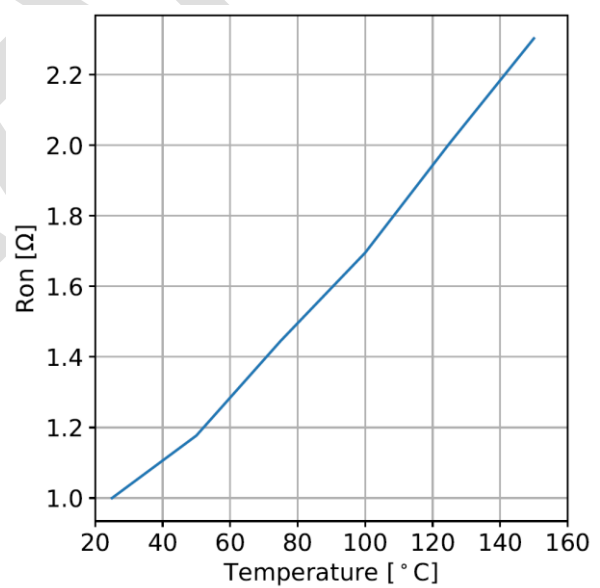
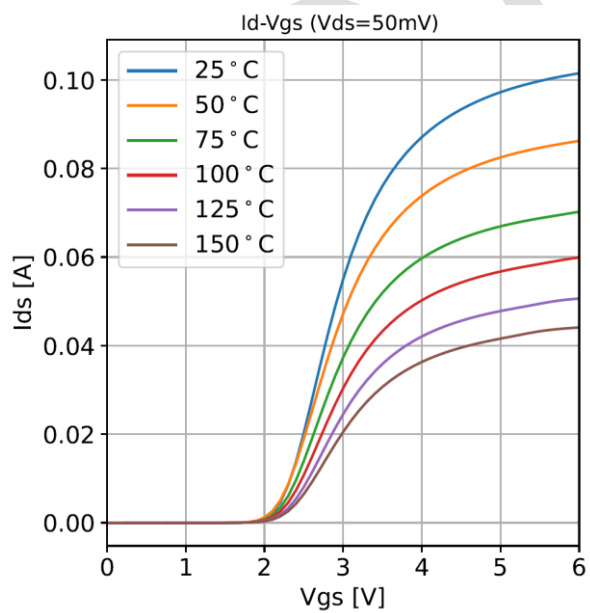
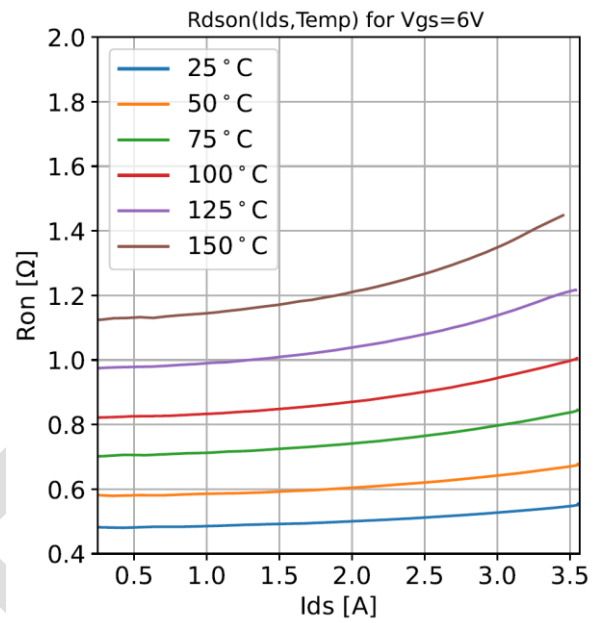
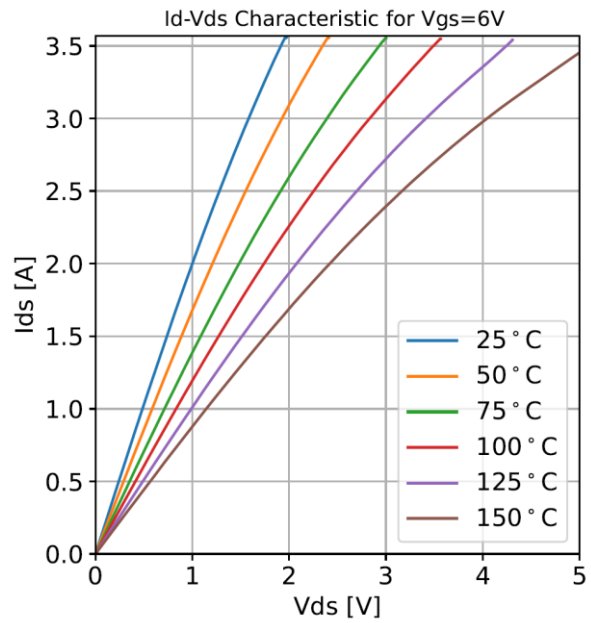
**Electrical Characteristics** (Typical Values @  $T_J = 25^\circ\text{C}$  unless otherwise noted)

**Table 3**

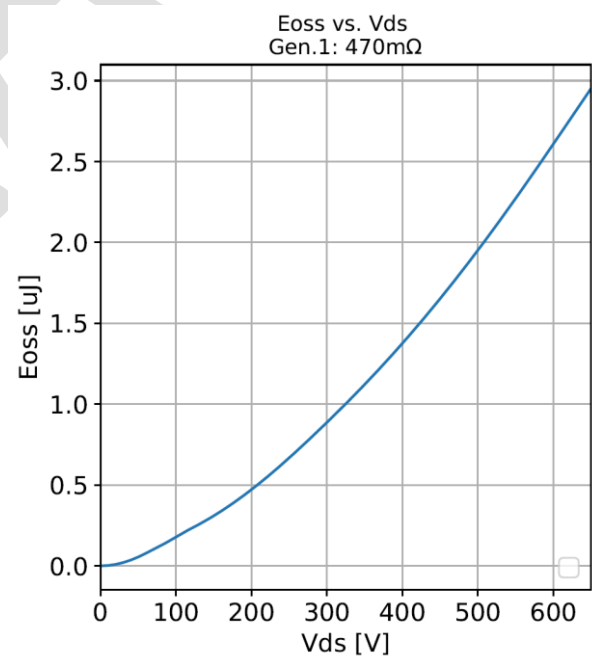
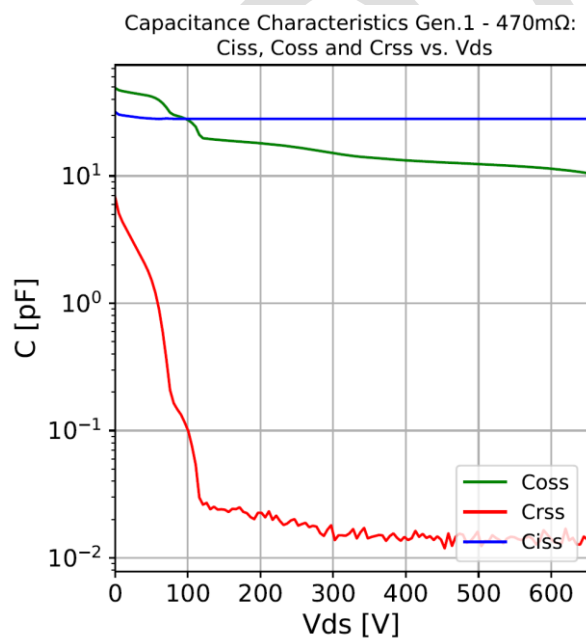
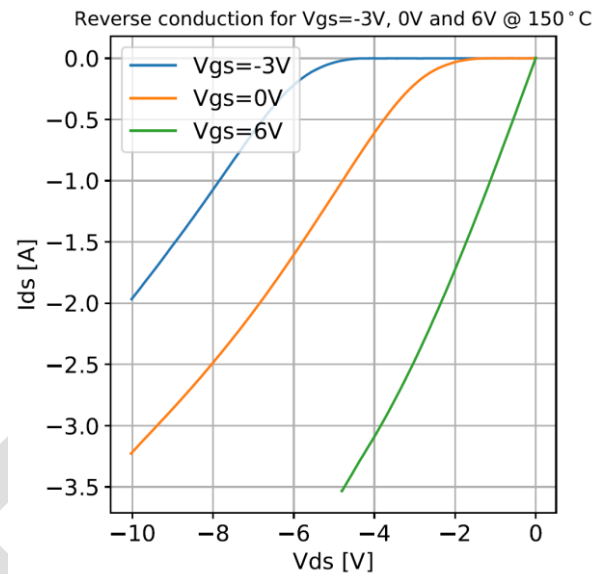
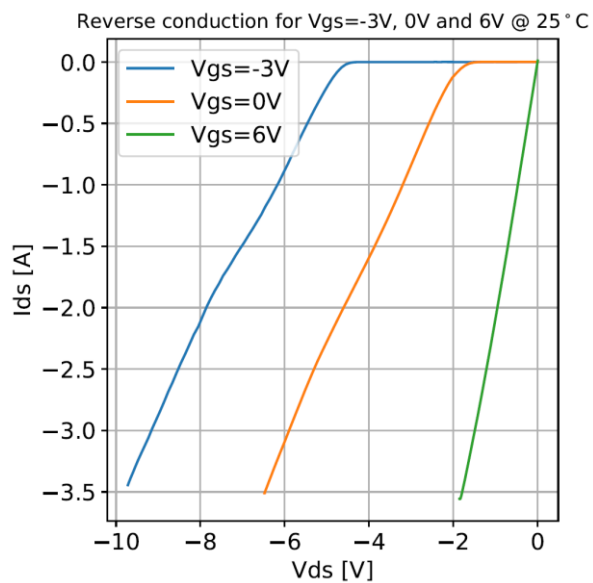
| Parameter                                    | Condition  | Symbol      | Min | Typ  | Max | Unit          |
|--|--|-------------|-----|------|-----|---------------|
| Drain to Source Blocking Voltage             | $V_{GS} = 0 \text{ V}$ , $I_{DSS} \leq 18 \mu\text{A}$                           | $V_{BDSS}$  | 650 |      |     | V             |
| On Resistance                                | $V_{GS} = 6 \text{ V}$ , $I_{DS} = 1 \text{ A}$                                  | $R_{DSon}$  |     | 470  | 640 | m $\Omega$    |
| Gate Threshold Voltage                       | $V_{DS} = V_{GS}$ , $I_{DS} = 0,6 \text{ mA}$                                    | $V_{Th}$    | 0.9 | 2.0  | 3.0 | V             |
| Gate to Source Current                       | $V_{GS} = 6 \text{ V}$ , $V_{DS} = 0 \text{ V}$                                  | $I_{GS}$    |     | 100  |     | $\mu\text{A}$ |
| Drain to Source Leakage Current              | $V_{DSS} = 650 \text{ V}$ , $V_{GS} = 0 \text{ V}$                               | $I_{DSS}$   |     | 0,2  |     | $\mu\text{A}$ |
| Input Capacitance                            | $V_{DS} = 400 \text{ V}$<br>$V_{GS} = 0 \text{ V}$<br>$f = 100 \text{ kHz}$      | $C_{ISS}$   |     | 25   |     | pF            |
| Output Capacitance                           |  | $C_{OSS}$   |     | 13   |     | pF            |
| Reverse Transfer Capacitance                 |  | $C_{RSS}$   |     | 0,02 |     | pF            |
| Output Charge                                | $V_{DS} = 400 \text{ V}$ , $V_{GS} = 0 \text{ V}$                                | $Q_{OSS}$   |     | 7,5  |     | nC            |
| Output Cap stored energy                     | $V_{DS} = 400 \text{ V}$<br>$V_{GS} = 0 \text{ V}$ , $f = 100 \text{ kHz}$       | $E_{OSS}$   |     | 1,2  |     | $\mu\text{J}$ |
| Total Gate Charge                            | $V_{ds} = 0 \text{ to } 400 \text{ V}$ ,<br>$V_{gs} = 0 \text{ to } 6 \text{ V}$ | $Q_g$       |     | 0,7  |     | nC            |
| Effective Output Capacitance, Energy related | $V_{ds} = 0 \text{ to } 400 \text{ V}$ ,<br>$V_{gs} = 0 \text{ V}$               | $Co_{(er)}$ |     | 15   |     | pF            |
| Effective Output Capacitance, Time related   | $V_{ds} = 0 \text{ to } 400 \text{ V}$ ,<br>$V_{gs} = 0 \text{ V}$               | $Co_{(tr)}$ |     | 19   |     | pF            |

**Note:** Figures are based on a linear scaling of the 120 m $\Omega$  transistor

## Electrical Graphs (1/2)



## Electrical Graphs (2/2)



## Test Circuits

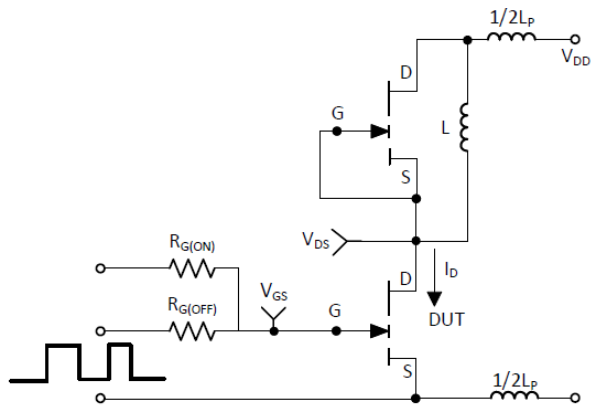


Fig 13: Switching Test Circuit

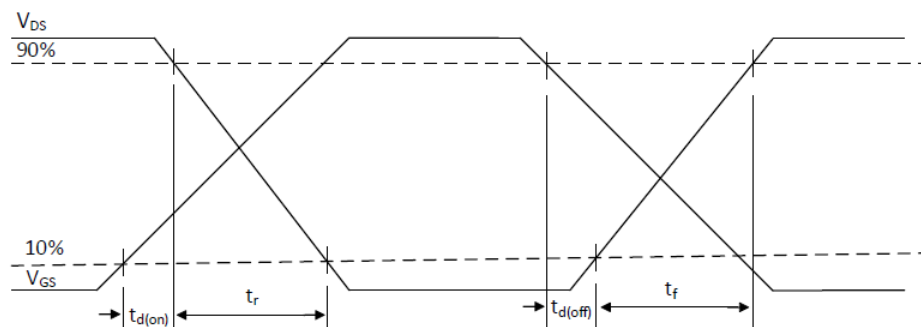


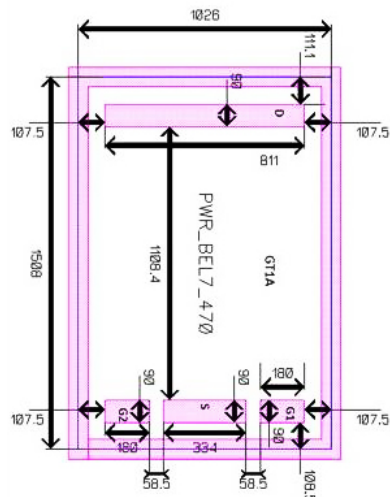
Fig 14: Switching Time Waveforms

## Package Information

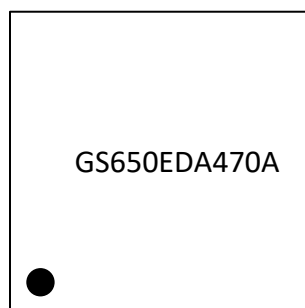
### Bare Die

Dimensions of the pads in  $\mu\text{m}$  refer to the passivation and polyimide opening.

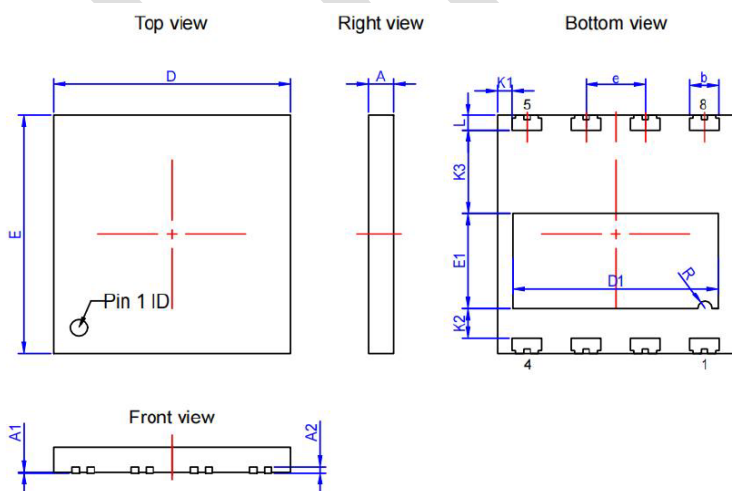
Drawing is not to scale.



### Marking

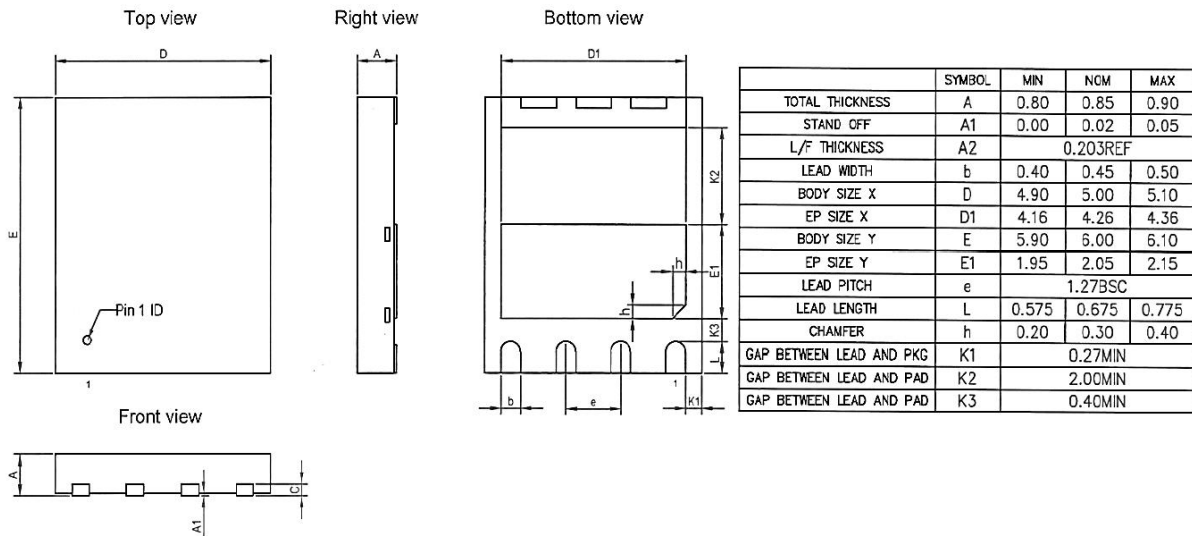


### DFN 8x8



|                 | SYMBOL | MIN  | NOM      | MAX  |
|-----------------|--------|------|----------|------|
| TOTAL THICKNESS | A      | 0.75 | 0.85     | 0.95 |
| STAND OFF       | A1     | 0.00 | 0.03     | 0.05 |
| L/F THICKNESS   | A2     |      | 0.203REF |      |
| LEAD WIDTH      | b      | 0.95 | 1.00     | 1.05 |
| BODY SIZE X     | D      | 7.90 | 8.00     | 8.10 |
| EP SIZE X       | D1     | 6.84 | 6.94     | 7.04 |
| BODY SIZE Y     | E      | 7.90 | 8.00     | 8.10 |
| EP SIZE Y       | E1     | 3.10 | 3.20     | 3.30 |
| LEAD PITCH      | e      |      | 2.00BSC  |      |
| SPACING         | K1     | 0.40 | 0.50     | 0.60 |
| SPACING         | K2     | 0.90 | 1.00     | 1.10 |
| SPACING         | K3     | 2.70 | 2.80     | 2.90 |
| LEAD LENGTH     | L      | 0.40 | 0.50     | 0.60 |
| RADIUS          | R      | 0.15 | 0.25     | 0.35 |

## DFN 5x6



### Disclaimer

This Product Sample is not a finished product and is not available for sale to consumers. The Product Sample is only intended for research, development, demonstration, and evaluation purposes and will only be used in laboratory/development areas by persons with an engineering/technical training and familiar with the risks associated with handling electrical/mechanical components, systems and subsystems. These persons assume full responsibility/liability for proper and safe handling of the Product Sample. Any other use, resale or redistribution of the Product Sample for any other purpose is strictly prohibited.